# Memory Chips with Adjustable Configurations

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**Abstract**

In this paper, we present the concept of Field Programmable Memory Cell Arrays (FPMCAs) as the memory counterpart to Field Programmable Gate Arrays which have proved their utility in design and rapid prototyping. Principles of dynamic reconfigurability using programmable logic and programmable interconnect are incorporated into random access memories to achieve this flexibility. We first present the design of a variable width RAM (VaWiRAM) which is a simple example of a Field Programmable Memory Cell Array. The configuration of VaWiRAMs can be adjusted by setting a few configuration pins on the memory chip. A VaWiRAM reconfigurable between widths 1 and $W_{max}$ can be constructed with the extra cost of $W_{max} - 1$ pass gates, $\frac{W_{max}}{2}$ 2-to-1 multiplexers, and $\lceil log_2[log_2(k) + 1] \rceil$ mode pins. A novel scheme to overlap the address pins with mode control pins and achieve the mode control with only one extra pin is also presented. The paper discusses the architecture of the proposed VaWiRAMs in detail, analyzes the design tradeoffs and introduces the concept of FPMCAs.

**Keywords:** Dynamically alterable memory configurations, Flexible Memory, Random Access Memory, Reconfigurable Memory.

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