IISWC 2020 Tutorial: Proxy Benchmarks for Reproducible Research

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UT Austin
&
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Outline

- Introduction to Proxy Benchmarks
  - Miniaturization, Software Stack Abstraction, Proprietary Codes
- Metrics, Techniques and Results for early Proxies
  - Bell, Joshi, Ganesan, and Panda Proxies; Results
- SimPoint as an alternative (CPU 2017 SimPoints) – Steven Flolid
- Challenges - Improving Accuracy of Proxy Benchmarks
  - Branch and Memory Behavior – Problem and Current State
  - Presentations by Zachary Susskind and Steven Flolid
- Industry Use
  - Intel – Presentation from Emily Shriver
- ISA Independence - LLVM Proxies
- Reproducibility of Research using Proxies
- Other Applications of Proxy Code Generator
Introduction

- Bad Press on Early Synthetic Benchmarks
- Whetstone, Dhrystone
- Misuse of Synthetic Benchmarks
- Not many good memories
- A totally new look at a new kind of synthetic benchmarks
- A few new scenarios
  - The Pre-Silicon Nightmare
  - Proprietary Applications that cannot be shared
  - Expiring Benchmarks
  - Power and Thermal Stress Benchmarks
The Presilicon Design Nightmare

Modern microprocessors are built from millions of lines of VHDL/Verilog code and billions of transistors.

RTL and Performance Models are 1000X or more slower than hardware.

Industry standard benchmarks run for hours on actual hardware.

Design tradeoffs need to be analyzed quickly to make timely design decisions.

If the wrong decisions are made, the presilicon nightmare will become a serious postsilicon nightmare.
Methodology: Workload Modeling and Synthesis

1. Identify a list of intrinsic properties $\alpha, \beta, \gamma \ldots \omega$ to uniquely describe the behavior of a modern program

2. Develop a methodology to reproduce the same behavior synthetically
Representing a Program with Intrinsic Properties

- Is it possible to find a list of intrinsic properties $\alpha, \beta, \gamma, \ldots \omega$ to uniquely describe a program?

- What will be the characteristics $\alpha, \beta, \gamma, \ldots \omega$?

- Platform (Micro-architecture) Independent Characteristics
  - i-mix, locality, address patterns, dependency

- Platform (Micro-architecture) Dependent Characteristics
  - Cache-hit rates, IPC/throughput, coherency traffic
Proxy Workload Generation

Workload Space of Inherent Program Characteristics

Modeling Workload Attributes into Synthetic Workload

Experiment Environment

Workload Signature = Point in Workload Space

Workload Synthesizer

Synthetic Benchmark Clone

VHDL/Verilog Models

Performance Simulator

Instruction Mix

Control Flow Behavior

Program Locality

Instruction Level Parallelism
Miniaturized Proxy Generation Process

Real Workload

Instruction Mix, ILP, Data Access Patterns, branch patterns ..

Measure Workload Characteristics at Basic Block Granularity

Detailed Workload Profile

Synthetic Clone

Generate Synthetic Clone with Similar Inherent Characteristics

ADD R1, R2, R3
LD R4, R1, R6
MUL R3, R6, R7
ADD R3, R2, R5
DIV R10, R2, R1
SUB R3, R5, R6
STORE R3, R10, R20
ADD R1, R2, R3
LD R4, R1, R6
MUL R3, R6, R7
ADD R3, R2, R5
DIV R10, R2, R1
SUB R3, R5, R1
BEQ R3, R6, LOOP
SUB R3, R5, R6
STORE R3, R10, R20
DIV R10, R2, R1
..........
Steps in Proxy generation

- Generate Workload profile
  - Command: `./mkJSON_both.sh $input $output $output_name.fixed`

- Generate Proxy
  - Command: `./CodeGenarator.py --configFile=$file -o $output`

- Run Proxy
  - Command: `c executable`
Statistical Flow Graph (SFG)
## Profiling the Original Workload

<table>
<thead>
<tr>
<th>No.</th>
<th>Metric</th>
<th>Category</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Dynamic execution freq. of basic blocks</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Average basic block size</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Branch taken rate for each branch</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Instruction pattern in a basic block</td>
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<tr>
<td>5</td>
<td>Branch transition rate for each branch present in the workload</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>% Integer multiplication</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>% Integer division</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>% FP multiplication</td>
<td>Instruction mix</td>
</tr>
<tr>
<td>9</td>
<td>%FP division</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>% Loads</td>
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</tr>
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<td>11</td>
<td>% Stores</td>
<td></td>
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<td>12</td>
<td>% Branches</td>
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<tr>
<td>13</td>
<td>Dependency distance distribution per instruction type</td>
<td>Instruction level parallelism</td>
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<tr>
<td>14</td>
<td>Stride value per static load/store</td>
<td>Data locality</td>
</tr>
<tr>
<td>15</td>
<td>Data Footprint of the workload</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Mean and standard deviation of the MLP</td>
<td>Memory level parallelism</td>
</tr>
<tr>
<td>17</td>
<td>Mean number of consecutive dynamic inst. when no outstanding long-latency loads</td>
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<tr>
<td>No.</td>
<td>Metric</td>
<td>Category</td>
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<td>------------------------------------------------------------------------</td>
<td>-----------------------------------------------</td>
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<tr>
<td>1</td>
<td>Basic block size</td>
<td>Control flow predictability</td>
</tr>
<tr>
<td>2</td>
<td>Branch taken rate for each branch</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Branch transition rate</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Proportion of INT ALU, INT MUL, INT DIV, FP ADD, FP MUL, FP DIV, FP MOV, FP SQRT, LOAD &amp; STORE</td>
<td>Instruction mix</td>
</tr>
<tr>
<td>5</td>
<td>Dependency distance distribution</td>
<td>Instruction level parallelism</td>
</tr>
<tr>
<td>6</td>
<td>Private stride value per static load/store</td>
<td>Data locality</td>
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<td>7</td>
<td>Data Footprint of the workload</td>
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</tr>
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<td>8</td>
<td>Mean and standard deviation of the MLP</td>
<td>Memory Level Parallelism (MLP)</td>
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<td>9</td>
<td>MLP frequency</td>
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<td>10</td>
<td>Number of threads</td>
<td>Thread level parallelism</td>
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<td>11</td>
<td><strong>Thread class and processor assignment</strong></td>
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<tr>
<td>12</td>
<td><strong>Percentage loads to private data</strong></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td><strong>Percentage loads to read-only data</strong></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td><strong>Percentage migratory loads</strong></td>
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</tr>
<tr>
<td>15</td>
<td><strong>Percentage consumer loads</strong></td>
<td>Shared data access pattern and communication characteristics</td>
</tr>
<tr>
<td>16</td>
<td><strong>Percentage irregular loads</strong></td>
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</tr>
<tr>
<td>17</td>
<td><strong>Percentage stores to private data</strong></td>
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</tr>
<tr>
<td>18</td>
<td><strong>Percentage producer stores</strong></td>
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</tr>
<tr>
<td>19</td>
<td><strong>Percentage irregular stores</strong></td>
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</tr>
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<td>20</td>
<td>Shared stride value per static load/store</td>
<td>Synchronization Characteristics</td>
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<td>21</td>
<td>Data pool distribution based on sharing patterns</td>
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<tr>
<td>22</td>
<td>Number of lock/unlock pairs and</td>
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</tr>
<tr>
<td>23</td>
<td>Number of mutex objects</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Number of Instructions between lock and unlock</td>
<td></td>
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</tbody>
</table>
Instruction Dependency Distance

- **Instruction level parallelism:**
  - Lower dependency distance corresponds to lower ILP and vice versa.

```
ADD R1, R3, R4
MUL R5, R3, R2
ADD R5, R3, R6
LD R4, (R1)
SUB R8, R2, R1
```

Read After Write Dependency Distance = 3
# CFG Information - SPEC CPU2006

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>No. of B.Blks</th>
<th># B.Blks for 90% of Prog Exec.</th>
<th>Branch Transition Rate</th>
<th>Average B.Blk Size</th>
<th>Average Number of Succ. B.Blks</th>
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<tbody>
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<td>12.76</td>
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</table>
### CFG Information – Implant Bench

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>No. of B.Blks</th>
<th># B.Blks for 90% of Prog. Exec.</th>
<th>Branch Transition Rate</th>
<th>Average B.Blk Size</th>
<th>Average # of Succ. B.Blks</th>
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<tbody>
<tr>
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<td>1.91</td>
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<td>Genomics_NJ</td>
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<td>7</td>
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<td>1.76</td>
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</tbody>
</table>

- **Dynamic number of instructions varies from hundreds million to few thousands**
Workload Synthesis Framework
Workload Synthesis Algorithm

1. Generate program spine using basic block information.

2. Populate basic block with instructions satisfying target IMIX.
   - Model inter-instruction dependencies
     - Assign producer-consumer chains

3. Model inter-instruction dependencies
   - Model branch predictability
     - Insert test operation before every branch instruction to control branch outcome

4. Memory instruction stride/offset assignment
   - Stride-based memory model

5. Code generation
   - GCC inline assembly for x86

6. C code with embedded assembly instructions
   - Outer loop controls the # of dynamic instructions
   - Inner loop iterations control the data footprint

Outer-loop starts
Reset data arrays

ld
add
sub
br

add
sub
ld
mul
br

ld
st
br

Outer-loop
End BB
Code Generation

- **Step 1:**
  - Usage of two loops
  - Based on Instruction footprint of original, fix the number of basic blocks in the synthetic
Step 2: For each Basic Block

- Choose the instruction pattern from a pool of instruction patterns based on the frequency in the profile in terms of Instruction type
- If not use BB size and global Instruction mix
Step 3: Bind the basic blocks together using conditional jumps

- Low Transition Rate -> always taken/not taken
- Group into pools & use modulo operations

10.3%
\begin{align*}
\text{a,fa,m,m,a,ld,st,Br} \\
\text{TR: 0.15}
\end{align*}

23.1%
\begin{align*}
\text{m,m,ld,a,a,Br} \\
\text{TR: 0.07}
\end{align*}

2.5%
\begin{align*}
\text{a,x,ld,ld,ld,s,s,Br} \\
\text{TR: 0.08}
\end{align*}

13.2%
\begin{align*}
\text{a,fa,a,a,a,ld,st,Br} \\
\text{TR: 0.01}
\end{align*}

50.9%
\begin{align*}
\text{a,fm,a,m,m,ld,ld,ld,a,a,Br} \\
\text{TR: 0.44}
\end{align*}
Code Generation

- **Step 4: For each instruction**
  - Find a producer instn to assign a register dependency
  - Not compatible? Move up/down
Step 5: Assign registers

- Destination registers – RoundRobin
- Source registers – based on dependency
Step 6: Memory access model

- Ld/st access a set of 1-D arrays in a strided fashion.
- Ld/St - group into pools, assign array, 1 address calc instruction.
- Pointers - top of array at end of inner loop when required data footprint is touched.

Diagram showing different memory access patterns and their corresponding usage percentages and instructions.
Step 6: MLP model

- Load-Load dependencies
- Placement of highly strided loads
- For very infrequent highly bursty long latency loads, only 1 loop has all the long latency loads
Performance Results from Early Proxies

Bell: Some microarch dependent metrics; Strides computed based on measured cache miss rates

Average Error of 6.3% & Maximum Error of 9.9% (mcf) [Bell05,06]
Overall Power Estimation

Power Results from Bell Proxies

Average Error of 7.3% & Maximum Error of 10.6% (mcf)
## Five Orders of Magnitude Speedup!

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Speedup from Synthetic Benchmark Clone</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applu</td>
<td>22,300</td>
</tr>
<tr>
<td>apsi</td>
<td>34,700</td>
</tr>
<tr>
<td>art</td>
<td>4,500</td>
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<tr>
<td>bzip2</td>
<td>12,800</td>
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<tr>
<td>crafty</td>
<td>19,100</td>
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<tr>
<td>eon</td>
<td>8,000</td>
</tr>
<tr>
<td>equake</td>
<td>13,100</td>
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<td>gcc</td>
<td>4,600</td>
</tr>
<tr>
<td>gzip</td>
<td>10,300</td>
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<tr>
<td>mcf</td>
<td>6,100</td>
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<td>mesa</td>
<td>14,100</td>
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<td>mgrid</td>
<td>41,900</td>
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<td>swim</td>
<td>22,500</td>
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<td>twolf</td>
<td>34,600</td>
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<tr>
<td>vortex</td>
<td>11,800</td>
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<td>vpr</td>
<td>8,400</td>
</tr>
<tr>
<td>wupwise</td>
<td>34,900</td>
</tr>
</tbody>
</table>
Improvements from Joshi and Ganesan

- Joshi added the following metrics:
  - Branch Transition Rate
  - Data Reuse Distance
- Ganesan added the following metrics:
  - MLP (Memory Level Parallelism)
  - Parallel Code Data sharing and Synchronization Metrics
Previous approaches and Memory Level Parallelism

- Existing synthetic workload generation methodologies Joshi et al [IISWC 06], Bell et al [ISPASS ’06, ICS ’05]
  - Capture control flow, cache access and ILP behavior
  - Do not capture the burstiness of long-latency loads or the Memory Level Parallelism (MLP)
  - May still match the missrate of the original, but not the performance
Memory Level Parallelism
- MLP Aware - Avg = 2.8%, Max = 7.7% for 464.h264ref
- MLP Unaware – Avg = 15.3%
IPC Comparison – ImplantBench

- Avg = 2.9%, Max = 7.2%
Power Comparison

Power Comparison

Power per cycle (W)

Orig
MLP aware synth
MLP unaware synth

Avg = 14%

Avg = 2.5%

ImplantBench

Power per cycle (W)

Orig
MLP aware synth
MLP unaware synth

Avg = 14%

Avg = 2.5%
Relative IPC Accuracy for CINT2006 Benchmarks

**462.libquantum**

- IPC vs. Machine configurations
- Y-axis: IPC
- X-axis: Machine configurations (RUU 0.5x, RUU 0.25x, LSQ 0.5x, LSQ 0.25x, BTB 2x, Comb BP, L2 size 0.5x, L2 Assoc 2x, L1 size 2x, Iss. Width 2x, Dec. Width 2x, Com. Width 2x, Baseline)
- Data points for Orig and Synth

**471.omnetpp**

- IPC vs. Machine configurations
- Y-axis: IPC
- X-axis: Machine configurations (RUU 0.5x, RUU 0.25x, LSQ 0.5x, LSQ 0.25x, BTB 2x, Comb BP, L2 size 0.5x, L2 Assoc 2x, L1 size 2x, Iss. Width 2x, Dec. Width 2x, Com. Width 2x, Baseline)
- Data points for Orig and Synth
Relative Power Accuracy for CPU2006

**462.libquantum**

![Graph showing power per cycle (W) for various machine configurations for 462.libquantum.]

**433.milc**

![Graph showing power per cycle (W) for various machine configurations for 433.milc.]

Lizy K. John, LCA, UTAustin

10/26/20
Performance Proxies for Big Data Workloads

- Web Browsers
- Mobile Devices
- Personal Computers
- Device Specific Renderers
- HTML, JavaScript, etc.

Business Logic Layer

Data Access Layer, Load Balancing

- SQL / NoSQL Server Drivers
- Database Drivers
- XML Query
- File System Query

Database Server
- Database
- XML Storage
- File System

Operating System
Instruction-level Profiling Impractical; Estimate METRICS from Perf Counters

- **Instruction-mix**
  - Measured using hardware performance counters
  - Fraction of integer (INT) ALU, INT MUL, INT DIV, floating-point (FP) ADD, FP DIV, FP MUL, loads, stores, control-flow instructions.

- **Instruction footprint**
  - Derived based on the instruction cache miss rate of the original application on a default instruction cache size (64KB, 64B line-size, 2-way set-associative).

- **Average basic-block size**
  - Estimated based on the instruction count and control instruction mix metrics.
Instruction-level METRIC Estimation (Contd)

- **Instruction level parallelism:**
  - Modeled by controlling the dependency distance (DD) between instructions.
  - Lower dependency distance corresponds to lower ILP and vice versa.

```
ADD R1, R3, R4
MUL R5, R3, R2
ADD R5, R3, R6
LD R4, (R1)
SUB R8, R2, R1
```

Read After Write Dependency Distance = 3

- Avg DD estimated based on the fraction of dependency-related stall events (measured using hardware performance counters) of an application.
Memory-access characteristics

- Original approach – PIN-based memory locality characterization
  - Local Stride - Per ld/st stride distribution
  - Global Stride – Stride distribution of the global memory access streams
- Perf Counter Approach: Strides estimated based on the data cache miss rates of the original application.
  - E.g., 50% hit-rates can be modeled using a stride of 8 (assuming 64B cache-line size)
CONTROL-FLOW BEHAVIOR

- Branch predictability (BP) of the original application is measured using the branch prediction rate.
- A branch instruction's predictability can be controlled using its transition frequency.
  \[
  \text{Branch Transition Rate} = \frac{\# \text{ of Taken} - \text{Not Taken transitions}}{\# \text{ of times executed}}
  \]
- PerfProx estimates the fraction of control instructions in the proxy benchmark that will have a particular predictability behavior.
  Find the set of \( f_i \) such that
  \[
  \text{BP} = f_1 \ast 1 + f_2 \ast 0.5 + f_3 \ast 0.33 + \ldots
  \]
- Assuming a 2-bit saturating counter based branch predictor, \( f_1, f_2, f_3 \ldots \) are the fraction of branches with 100\% (TTTTTTTT or NNNNNNNN), 50\% (TNTNTNTN), 33\% (TTNTNTTNTT) predictability respectively.
System CALL Activity

- Many emerging big-data applications spend a significant fraction of their execution time (upto 30%) executing operating system (OS) code.

- System activity monitored using STRACE tool and the fraction of user-mode and kernel-mode instructions using hardware performance counters.

- Modeled by inserting target fraction of system calls into the basic blocks in the proxy benchmark.
DATABASE PROXY EVALUATION

• Databases - Cassandra, MongoDB and MySQL

• Benchmarks
  • Data analytics (TPC-H Benchmarks) - 10GB, Full runs of Q1, Q3, Q6, Q14 and Q19.
  • Data serving (Yahoo! Cloud Serving Benchmark, YCSB) – 12GB, 100 Million operations.

• Performance monitoring performed on real systems using Linux Perf tool.

• Average instruction-count of the generated proxy benchmarks is ~2 billion (~520 times smaller than original database applications).

<table>
<thead>
<tr>
<th>Configuration</th>
<th>System-A</th>
<th>System-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Architecture</td>
<td>64-bit processor, Core micro-architecture</td>
<td>64-bit processor, Ivy-bridge micro-architecture</td>
</tr>
<tr>
<td>Core Frequency</td>
<td>2 GHz</td>
<td>2.50 GHz</td>
</tr>
<tr>
<td>Cache Configuration</td>
<td>Private L1 caches (64 KB I and D caches), 12 MB L2 cache</td>
<td>Three levels of caches, 1.5MB L2, 15MB L3 cache</td>
</tr>
<tr>
<td>Memory</td>
<td>16 GB DRAM</td>
<td>64 GB DRAM</td>
</tr>
</tbody>
</table>
The proxy benchmarks mimic the IPC of the original applications with 94.9% (avg) accuracy for data-serving applications and 93.5% (avg) accuracy for data-analytics applications.
Performance VALIDATION ON system-A

- Branch Prediction Rate
- Normalized L1 miss rate
- %OS, %user IMIX

- Actual
- Proxy
- Error

- ρ = 0.99
- ρ = 0.937
- ρ = 0.967
Correlation between the average power consumption of the proxy and actual applications is high (0.97).
PERFORMANCE CROSS-VALIDATION ON system-B

Cassandra YCSB

MongoDB YCSB

MySQL TPC-H

Mon-WLA Mon-WLB Mon-WLC Mon-WLD

TPC-H Q1 TPC-H Q3 TPC-H Q6 TPC-H Q14 TPC-H Q19

ρ = 0.92

ρ = 0.93

ρ = 0.88

Lizy K. John, LCA, UTAustin
SUMMARY OF ORIGINAL TO PROXY COMPARISON

Cassandra-ORIG

Cassandra-Proxy

MongoDB-ORIG

MongoDB-Proxy

MySQL-ORIG

MySQL-Proxy
Where to find proxies

- Github repository with most up to date proxies: https://github.com/UT-LCA/Proxy-Benchmarks

- Proxies are all c programs that can be compiled with GCC
  - Example: gcc Deepsjeng.c –o Deepsjeng.o

- Performance counters can be gathered with perf or other tools
  - Example: perf Deepsjeng.o
Cannot retrieve the latest commit at this time.

..

- Big_Data_Benchmarks
- CPU_2017
Cannot retrieve the latest commit at this time.

..

- proxy_cas_wc.c
- proxy_cas_wc_sys.c
- proxy_cas_wd.c
- proxy_mongowa.c
- proxy_mongowb.c
- proxy_tpcq1.c
- proxy_tpcq14.c
- proxy_tpcq19.c
- proxy_tpcq3.c
- proxy_tpcq6.c
Cannot retrieve the latest commit at this time.

- deepsjeng.c
- exchange2.c
- gcc.c
- leela.c
- mcf.c
- omnetpp.c
- perl.c
- x264.c
- xalancbmk.c
- xz.c
SPEC’17 BENCHMARK OVERVIEW

• CPU2017 Benchmark Overview
  • 43 Benchmarks: Speed & Rate versions of INT and FP programs

• CPU2017 vs CPU2006 Runtime Comparison

<table>
<thead>
<tr>
<th>Runtime Chars.</th>
<th>SPEC CPU2017</th>
<th>SPEC CPU2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Inst. Count</td>
<td>7,876,399,266,409</td>
<td>1,896,452,771,834</td>
</tr>
<tr>
<td>Total run time (all benchmarks)</td>
<td>72, 299 seconds</td>
<td>9860 seconds</td>
</tr>
</tbody>
</table>
## Benchmark Characteristics

<table>
<thead>
<tr>
<th>Benchmark name</th>
<th>Language</th>
<th>KLoC</th>
<th>Application area</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_s</td>
<td>C</td>
<td>362</td>
<td>Perl interpreter</td>
</tr>
<tr>
<td>Deepsjeng_s</td>
<td>C++</td>
<td>10</td>
<td>Artificial intelligence: alpha beta tree search (chess)</td>
</tr>
<tr>
<td>Omnetpp_s</td>
<td>C++</td>
<td>134</td>
<td>Discrete event simulation – computer network</td>
</tr>
<tr>
<td>Gcc_s</td>
<td>C</td>
<td>1304</td>
<td>GNU C compiler</td>
</tr>
<tr>
<td>Leela_s</td>
<td>C++</td>
<td>21</td>
<td>Artificial intelligence: Monte carlo tree search (Go)</td>
</tr>
</tbody>
</table>
## Benchmark Characteristics

<table>
<thead>
<tr>
<th>Benchmark name</th>
<th>Language</th>
<th>KLoC</th>
<th>Application area</th>
</tr>
</thead>
<tbody>
<tr>
<td>xalanxbenchmark_s</td>
<td>C++</td>
<td>520</td>
<td>XML to HTML conversion via XLST</td>
</tr>
<tr>
<td>mcf_s</td>
<td>C</td>
<td>3</td>
<td>Route Planning</td>
</tr>
<tr>
<td>x264_s</td>
<td>C</td>
<td>96</td>
<td>Video compression</td>
</tr>
<tr>
<td>exchange2_s</td>
<td>Fortran</td>
<td>1</td>
<td>Artificial Intelligence: recursive solution generator (Sudoku)</td>
</tr>
<tr>
<td>xz_s</td>
<td>C</td>
<td>33</td>
<td>General Data Compression</td>
</tr>
</tbody>
</table>
Proxy Performance (IPC)

Instructions Per Cycle (IPC)

- **orig**
- **proxy**
- **error**

Error percentages:
- 0.00%
- 5.00%
- 10.00%
- 15.00%
Proxy Performance (Power)

Running Average Power Limit (RAPL)

- orig
- proxy
- error
## Degree of Miniaturization

<table>
<thead>
<tr>
<th></th>
<th>perlbench</th>
<th></th>
<th>deepsjeng</th>
<th></th>
<th>omnetpp</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Orig</td>
<td>Proxy</td>
<td>Orig</td>
<td>Proxy</td>
<td>Orig</td>
<td>Proxy</td>
</tr>
<tr>
<td>#Dyn Instructions</td>
<td>1,283,859,685,081</td>
<td>630,103,279</td>
<td>2,275,616,966,086</td>
<td>671,753,323</td>
<td>1,102,787,632,966</td>
<td>608,628,244</td>
</tr>
<tr>
<td>Orig/Proxy # Instructions</td>
<td>2038</td>
<td></td>
<td>3388</td>
<td></td>
<td>1812</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>gcc</th>
<th></th>
<th>leela</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Orig</td>
<td>Proxy</td>
<td>Orig</td>
<td>Proxy</td>
</tr>
<tr>
<td>#Dyn Instructions</td>
<td>4,577,230,000,000</td>
<td>982,597,009</td>
<td>2,245,850,995,706</td>
<td>423,060,220</td>
</tr>
<tr>
<td>Orig/Proxy # Instructions</td>
<td>4658</td>
<td></td>
<td>5309</td>
<td></td>
</tr>
</tbody>
</table>

- All proxies have less than 1 billion dynamic instruction count
## Degree of Miniaturization

<table>
<thead>
<tr>
<th></th>
<th>xalanxbmk</th>
<th>mcf</th>
<th>x264</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Orig</td>
<td>Proxy</td>
<td>Orig</td>
</tr>
<tr>
<td>#Dyn Instructions</td>
<td>1,315,970,803,200</td>
<td>510,531,529</td>
<td>1,782,190,000,000</td>
</tr>
<tr>
<td>Orig/Proxy # Instructions</td>
<td><strong>2578</strong></td>
<td></td>
<td><strong>2257</strong></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>exchange2</th>
<th>xz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Orig</td>
<td>Proxy</td>
</tr>
<tr>
<td>#Dyn Instructions</td>
<td>6,643,720,000,000</td>
<td>895,456,832</td>
</tr>
<tr>
<td>Orig/Proxy # Instructions</td>
<td><strong>7419</strong></td>
<td></td>
</tr>
</tbody>
</table>

- all proxies have less than 1 billion dynamic instruction count
Control-flow Behavior

Comparing branch misprediction rate of ORIG and PROXY

Branch Misprediction Rate (%)
# Cache & TLB Performance (1/2)

<table>
<thead>
<tr>
<th></th>
<th>perlbench</th>
<th>deepsjeng</th>
<th>omnetpp</th>
<th>gcc</th>
<th>leela</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ORIG</strong></td>
<td>0.10</td>
<td>0.22</td>
<td>5.00</td>
<td>0.34</td>
<td>0.04</td>
</tr>
<tr>
<td><strong>PROXY</strong></td>
<td>0.01</td>
<td>0.01</td>
<td>0.09</td>
<td>0.02</td>
<td>0.02</td>
</tr>
<tr>
<td><strong>DTLB MPKI</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ORIG</strong></td>
<td>3.51</td>
<td>4.55</td>
<td>36.64</td>
<td>12.66</td>
<td>4.98</td>
</tr>
<tr>
<td><strong>PROXY</strong></td>
<td>4.77</td>
<td>7.30</td>
<td>32.88</td>
<td>10.05</td>
<td>4.25</td>
</tr>
<tr>
<td><strong>Dcache MPKI</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ORIG</strong></td>
<td>1.64</td>
<td>1.41</td>
<td>17.79</td>
<td>1.38</td>
<td>0.58</td>
</tr>
<tr>
<td><strong>PROXY</strong></td>
<td>0.00</td>
<td>0.02</td>
<td>13.74</td>
<td>4.99</td>
<td>0.01</td>
</tr>
<tr>
<td><strong>L2 MPKI</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ORIG</strong></td>
<td>0.01</td>
<td>1.10</td>
<td>6.31</td>
<td>0.62</td>
<td>4.61</td>
</tr>
<tr>
<td><strong>PROXY</strong></td>
<td>0.00</td>
<td>0.00</td>
<td>9.70</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td><strong>L3 MPKI</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ORIG</strong></td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
</tbody>
</table>
Cache & TLB Performance (2/2)

<table>
<thead>
<tr>
<th></th>
<th>X264</th>
<th>Exchange2</th>
<th>xz</th>
<th>xalanxbmk</th>
<th>mcf</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ORIG</td>
<td>PROXY</td>
<td>ORIG</td>
<td>PROXY</td>
<td>ORIG</td>
</tr>
<tr>
<td>DTLB MPKI</td>
<td>0.03</td>
<td>0.01</td>
<td>0.00</td>
<td>0.02</td>
<td>2.04</td>
</tr>
<tr>
<td>Dcache MPKI</td>
<td>1.44</td>
<td>0.58</td>
<td>0.02</td>
<td>1.38</td>
<td>16.06</td>
</tr>
<tr>
<td>L2 MPKI</td>
<td>0.34</td>
<td>0.33</td>
<td>0.00</td>
<td>0.74</td>
<td>5.00</td>
</tr>
<tr>
<td>L3 MPKI</td>
<td>0.10</td>
<td>0.15</td>
<td>0.00</td>
<td>0.00</td>
<td>0.87</td>
</tr>
</tbody>
</table>
SimPoint as an Alternative – UT LCA SimPoints

- **SIMPOINTS** are popularly used with simulators to reduce simulation time.

- UT Laboratory for Computer Architecture has generated SimPoints for SPEC CPU 2017

- **SimPoints for SPEC CPU 2017** are available at https://github.com/UT-LCA/Scalability-Phase-Simpoint-of-SPEC-CPU2017/releases
SimPoints

This folder holds the results of SimPoint study. Pinballs for SimPoints are available for download here.

Usage

Pinballs can be run natively using the Software Develop Emulator from Intel (https://software.intel.com/en-us/articles/intel-software-development-emulator). Gem5 (http://gem5.org/Simpoints) and Sniper (http://snipersim.org/w/Pinballs) also support the replaying of pinballs.

Interpreting the meaning of the 10 to 30 Pinballs for each workload in SPEC CPU 2017 is fairly straightforward. Each pinball base name specifies the key details for the pinball. An example is included below:
deejspjeng.test_38307_t0r1_warmup1501_prolog0_region100000038_epilog0_001_0-05045.0.address

The file has many parts to its name, each with a specific meaning.

"program name","run name","run number","t"thread number","r"region number","_warmup","num warm up instructions","_prolog","num prolog instructions","region","num instructions in region of interest","_epilog","num epilog instructions",""region number again",""thread number again","-"weight of the region".0."file type"
SimPoint as an Alternative

- Simpoint [1] breaks a workload into equal sized regions (100 Million Instructions)
- Regions are profiled based on micro-architecture independent Basic Block Vectors (BBV)
- Similar regions are clustered together based on the BBV using K-means
- A single region is simulated to represent each cluster

SimPoint Limitations

- Dominant region can vary significantly from average behavior

<table>
<thead>
<tr>
<th>Cluster ID</th>
<th>Cluster Weight</th>
<th>Representative Perf. Metric</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.87%</td>
<td>1.60</td>
</tr>
<tr>
<td>1</td>
<td>23.62%</td>
<td>1.21</td>
</tr>
<tr>
<td>2</td>
<td>1.36%</td>
<td>1.91</td>
</tr>
<tr>
<td>3</td>
<td>12.00%</td>
<td>1.47</td>
</tr>
<tr>
<td>4</td>
<td>0.09%</td>
<td>1.04</td>
</tr>
<tr>
<td>5</td>
<td>0.44%</td>
<td>1.47</td>
</tr>
<tr>
<td>6</td>
<td>0.69%</td>
<td>1.61</td>
</tr>
<tr>
<td>7</td>
<td>0.36%</td>
<td>1.46</td>
</tr>
<tr>
<td>8</td>
<td>0.84%</td>
<td>1.54</td>
</tr>
<tr>
<td>9</td>
<td>0.17%</td>
<td>1.33</td>
</tr>
<tr>
<td>10</td>
<td>3.60%</td>
<td>1.16</td>
</tr>
<tr>
<td>11</td>
<td>0.82%</td>
<td>1.74</td>
</tr>
<tr>
<td>12</td>
<td>5.28%</td>
<td>1.77</td>
</tr>
<tr>
<td>13</td>
<td>1.21%</td>
<td>1.41</td>
</tr>
<tr>
<td>14</td>
<td>48.65%</td>
<td>1.85</td>
</tr>
</tbody>
</table>

Weighted Sum

Simpoint Estimate: 1.61
SimPoints for CPU 2017

<table>
<thead>
<tr>
<th>Benchmarks</th>
<th>Simulation Points</th>
<th>90 percentile Points</th>
<th>Instructions (billions)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SPECs speed</td>
<td>Integer</td>
<td></td>
</tr>
<tr>
<td>600.perlbench_s</td>
<td>25</td>
<td>13</td>
<td>2696</td>
</tr>
<tr>
<td>602gcc_s</td>
<td>15</td>
<td>5</td>
<td>7226</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>21</td>
<td>11</td>
<td>1775</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>8</td>
<td>5</td>
<td>1102</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>14</td>
<td>9</td>
<td>12546</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>20</td>
<td>16</td>
<td>2250</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>29</td>
<td>21</td>
<td>2245</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>19</td>
<td>15</td>
<td>6643</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>21</td>
<td>15</td>
<td>8264</td>
</tr>
<tr>
<td><strong>Int Average</strong></td>
<td><strong>19.1</strong></td>
<td><strong>12.22</strong></td>
<td><strong>4607</strong></td>
</tr>
</tbody>
</table>

|                    | SPECs speed       | Floating-point       |                          |
| 603.bwaves_s       | 9                 | 3                    | 66395                    |
| 619.lbm_s          | 8                 | 4                    | 4416                     |
| 638.imagick_s      | 15                | 6                    | 66788                    |
| 644.nab_s          | 12                | 5                    | 13489                    |
| 649.fotonik3d_s    | 17                | 7                    | 4280                     |
| **FP Average**     | **12.2**          | **5**                | **24204**                |
## Multiple SimPoints

<table>
<thead>
<tr>
<th>Benchmarks</th>
<th>Start Instructions(100 million)/Weight(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.peribench_s</td>
<td>(214681/28.85, (924424/12.60, (1277200/8.97, (1327590/7.96, (58779/7.77, (54633/5.43, (521547/5.39, (1233410/3.88, (752064/2.42, (701679/2.40, (789265/2.19, (1258340/2.06, (236975/1.78, (48882/1.71, (482810/1.44, (467463/0.77, (478321/0.68, (29698/0.68, (199580/0.61, (607466/0.55, (236842/0.54, (1339730/0.53, (1044350/0.30, (790578/0.30, (1141890/0.23)</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>(23077/48.65, (35817/23.62, (21069/12.00, (28125/8.28, (29282/3.60, (1353/1.36, (35911/1.21, (34118/0.87, (24369/0.84, (33794/0.82, (33733/0.69, (36933/0.44, (27933/0.36, (27185/0.17, (910/0.09)</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>(5943/21.24, (16201/12.54, (6315/10.82, (14440/10.75, (587/7.69, (6563/6.97, (13680/6.04, (743/5.14, (14107/3.40, (12030/3.36, (12099/2.41, (9255/2.25, (7606/2.12, (14669/2.02, (7843/0.93, (15653/0.89, (12189/0.50, (17489/0.42, (9375/0.27, (15180/0.19, (1765/0.07)</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>(6053/32.56, (6737/30.32, (2966/15.25, (6239/0.00, (1387/6.55, (9548/5.76, (10990/0.51, (10994/0.06)</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>(49503/16.54, (22073/14.94, (3910/12.74, (42644/12.32, (10435/12.03, (46339/10.83, (26034/5.69, (41393/4.04, (11557/4.00, (24352/3.17, (4650/1.17, (1198/1.08, (53156/0.96, (31735/0.47)</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>(1709/8.84, (2185/7.87, (847/0.02, (9700/7.00, (2015/6.98, (6204/6.37, (637/5.85, (7853/5.74, (2054/5.69, (15965/5.60, (14515/5.28, (9851/5.05, (3602/4.01, (1215/3.94, (5259/3.73, (1183/2.92, (1134/2.76, (3900/2.53, (15357/2.39, (0/0.46)</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>(13198/8.63, (10150/7.15, (9272/6.85, (9870/6.75, (10635/6.57, (6871/5.64, (12252/5.49, (19208/4.29, (7341/4.17, (1830/3.90, (17685/3.67, (6004/3.59, (4934/3.45, (17328/3.37, (4952/3.10, (923/2.66, (21528/2.52, (1463/2.50, (22193/2.40, (1105/2.03, (820/1.91, (12296/1.84, (13929/1.60, (15764/1.47, (1193/1.36, (6041/1.15, (21296/0.98, (3514/0.96, (4/0.04)</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>(36567/13.00, (16895/9.39, (1400/8.92, (39442/8.76, (38731/6.97, (31742/6.59, (35941/6.33, (6913/5.80, (25357/5.25, (28962/4.09, (35764/3.86, (22587/3.21, (10870/3.02, (45973/2.94, (2995/2.88, (39598/2.72, (45675/2.26, (40484/2.04, (38264/1.88, (180/0.07, (44672/0.02)</td>
</tr>
<tr>
<td>603.bwaves_s</td>
<td>(59291/7.16, (248007/14.61, (28743/5.89, (31309/3.23, (31505/2.21, (95707/1.67, (31813/0.34, (26376/0.31, (30313/0.28)</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>(7134/69.69, (10742/14.92, (43825/4.43, (11740/4.36, (6240/3.65, (9400/2.38, (849/0.56, (0/0.01)</td>
</tr>
<tr>
<td>638.imagemick_s</td>
<td>(551856/43.83, (394592/27.24, (467091/8.12, (28460/4.97, (91452/4.24, (4209/2.76, (41027/2.50, (51582/2.45, (72623/1.27, (65600/1.21, (651005/0.78, (10504/0.54, (102890/0.04, (27272/0.04, (56740/0.04)</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>(9237/34.24, (52046/22.75, (56855/19.71, (58776/9.76, (12259/9.45, (13375/6.91, (48950/0.26, (12071/0.25, (13026/0.16, (10462/0.14, (7609/0.09, (84290/0.08)</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>(19088/43.91, (2468/29.02, (56395/6.90, (1608/4.72, (11626/2.65, (53620/2.21, (17985/2.12, (33097/1.95, (35644/1.20, (38568/0.91, (31846/0.83, (44869/0.83, (3563/0.80, (4626/0.64, (33943/0.49, (43842/0.41, (36949/0.41)</td>
</tr>
</tbody>
</table>
How to read the Table of Multiple SimPoints

<table>
<thead>
<tr>
<th>SimPoint</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>(214681/28.85)</td>
<td>(924424/12.60)</td>
<td>(789265/2.19)</td>
</tr>
<tr>
<td></td>
<td>(1258340/2.06)</td>
<td>(236842/0.54)</td>
<td>(1339730/0.53)</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>(23077/48.65)</td>
<td>(35817/23.62)</td>
<td>(36933/0.44)</td>
</tr>
<tr>
<td></td>
<td>(27933/0.36)</td>
<td>(271</td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>(5943/21.24)</td>
<td>(16201/12.54)</td>
<td>(63</td>
</tr>
<tr>
<td></td>
<td>(9255/2.25)</td>
<td>(7606/2.12)</td>
<td>(14669</td>
</tr>
</tbody>
</table>
In many cases, the dominant SimPoint has less than 10% weight

Proxies allow us to make a single proxy for the whole benchmark

Or

One proxy per SimPoint, giving more accuracy than the dominant SimPoint
Industry Use

IBM – 2006

AMD – 2010

Intel 2017-2019
Miniature Benchmarks for RTL Model Validations

Presentation by EMILY SHRIVER, Intel
Improving Accuracy of Proxies

- Current Challenges
  - Major Inaccuracies
  - Branch Behavior Capture
  - Memory Behavior Capture
Improving Branch Behavior

- Branch Profiling has become more precise in order to increase accuracy
  - Initially Global Transition Rate [1]
  - Added Global Taken Rate
  - Added Per Branch (local) Transition and Taken Rate
  - Added inter Branch Correlation [2]
  - Adding Variable inter Branch Correlation

Improving Branch Behavior

- Branch Profiling has become more precise in order to increase accuracy
  - Initially Global Transition Rate [1]
  - Added Global Taken Rate
  - Added Per Branch (local) Transition and Taken Rate
  - Added Inter-Branch Correlation [2]
  - Added Variable Inter-Branch Correlation

Proxy Branch Generation – Overview

- Branch mispredictions reduce overall IPC
  - Speculative work must be discarded

- Proxies should have branch predictor performance similar to original

- Metric of Interest: MPKI
  - Misses per thousand branch instructions
Profiling Branch Behavior

- Profile local behavior, i.e. per-static-branch
- Maintain a data structure for each static branch in the workload
- Every time a branch is encountered:
  - Increment the “encountered” count for the branch
  - If taken: increment the “taken” count for the branch
  - Compare taken behavior with the last time it was encountered
    • If different: increment the “transition” count for the branch
- Write raw results to file
- Discard data from extremely rare branches
  - 10% of static branches can make up 99.99% of dynamic branches
Profiling Branch Correlations

- Need to track a history of global branch behavior
  - Sliding window for last 512 global conditional branches

- Maintain a 512-entry table for each static branch

- Every time a branch \( b \) is encountered:
  - Compare “is_taken[\( b \)]” to all branches in window:
    - If \( \text{is\_taken}[\( b \)] \oplus \text{History}[i] \) then \( \text{Corr}[\( b \)][i] -= 1 \)
    - Else \( \text{Corr}[\( b \)][i] += 1 \)

- Normalize values to range \((-1, 1)\)
  - \( \text{Corr}[\( b \)][i] /= \text{Encountered}[\( b \)] \)

- Write to file; discard rare branches and weak correlations
Proxy Branch Generation

- **Use original static branches as “templates” for proxy branches**
  - Each proxy branch matches the taken and transition rates of its template

- **How many branches should use each template?**
  - Each proxy branch is dynamically executed the same number of times
  - Particularly common original branches should be used for multiple proxy branches
  - Scaling step automatically performed
Originally, we ordered branches randomly
  – This worked well in some cases, but clobbered correlations

So: Order branches to minimize correlation error
  – Currently, we just look at the strongest correlation
  – We also only consider the immediate previous branch
  – Error = \sum \text{abs}(\text{max}(\text{Corr}[b_n])) - \rho(b_n, b_{n-1})) \text{ for } n = 2, ..., N
  – Likely NP-hard; we don’t yet have a great heuristic
    • Still gives pretty good results!
Improving Memory Access Patterns

• The proxies in the repository use a stride based memory model that captures a per instruction memory pattern
  • Example: a load instruction accesses x3000, then x3008, x3010, x3018, ….

• Recent research (HALO) has found better accuracy through modeling[1]:
  • Intra-region stride locality
  • Inter-region reuse locality

• Developed proxies that implements these two techniques into proxies

HALO Memory Behavior

• For intra-region locality, a Markov chain is created for each region of memory to track patterns within.

• The probability of switching between regions is calculated for the inter-region reuse locality.

• HALO combines the intra-region locality and inter-region reuse distance to create similar memory traces.
HALO Memory Behavior

Figure 4: Intra-region locality profiling using cascaded stride tables (CSTs).
Leveraging Halo into Mind Prox

• The Markov tables can be used to create a set of traces for each region
  • This translates quite well to the large arrays already used in perfprox

• The inter region reuse locality translates to which arrays to access in which order
  • This can translate directly into accessing different arrays in an interleave that matches the Halo metrics

• Embedding the trace into a proxy was the last challenge
Challenge of Embedding Traces into Proxies

• Straight forward solution is to have an array of memory locations and read from the array to get the next address
  • This leads to an extra read to the array data structure

• The main challenge is overhead, any proxy technique for memory cannot have extra reads to a data structure
  • Why most proxies use stride-based techniques that slowly progress through memory
Linked List Solution

- Linked lists allow opportunity for arbitrary memory behavior without overhead
  - Walking a linked list updates the linked list pointer for every read
  - No useful information needs to be included in linked list, just the chain of pointers
  - Important step is converting a trace into a linked list format
Challenges with Linked Lists

- **Linked lists can only access an individual location once**
  - Many programs access locations repeatedly in a short period

- **Additionally, deciding how to deal with this issue leads to minimizing error between original trace and the linked list**
  - Accesses to same cache line can be seen as acceptable

- **Linked list can only handle reads, writes would clobber linked list**
  - Each node has a scratchpad for writing to instead of reading from
  - Thus writes are used to handle small offsets
Addressing the repeat access problem

- Most accesses to the same location are successive
  - From a stride perspective these would be approximately 0 offsets
- Small offsets are removed from the linked list and treated as stride accesses in the proxy
  - These would be memory accesses that do no update the linked list pointer
  - Currently all offsets less than 8 are removed
- Issue is also addressed by shortening memory trace
Reproducible Research

• We have developed a proxy generation methodology to generate miniature proxy benchmarks.
• Irrespective of the errors with their original counterparts, the proxies can be useful in reproducible research.
• Reproducibility is a problem in computer architecture research.
• Use these as benchmarks in architecture papers, and they can be used for validation when the next follow on work cannot fully simulate the earlier work completely due to simulator changes, runtime changes etc.
Reproducibility

- Reproducibility of Research using Proxies
  - Miniaturization Standpoint
  - Software Stack Abstraction Standpoint
  - Proprietary Codes Standpoint
  - Simulator Validation Standpoint

- Would like the research community to use the proxies along with other benchmarks
  - SPEC CPU 2017 Proxies
  - Data base (Cassandra, MongoDB, MySQL) Proxies
  - Github
ISA Independent Synthetic Benchmark Generation

- **Step 1: Generate synthetic code in LLVM IR**
  - Use Static Single Assigned (SSA) form
  - Not bounded to specific ISA
  - Targeting total number of dynamic instructions to desired value
- **Step 2: Create assembly for target ISAs**
  - Use modified LLVM backend
  - Disable optimization paths to preserve characteristics
- **Step 3: Compile binary for target ISAs**
  - Use general compiler for each ISAs
  - Does not require specialized tools
ISA Independent Synthetic Benchmarks

- **LLVM compiler infrastructure**
  - A virtual instruction set language
  - Various back-end support – x86, PowerPC, ARM, Alpha, SPARC, etc.

- **Use virtual ISA in SSA form**
  - Micro architecture independent
  - Avoid machine-specific optimizations in the front-end
  - Back-end takes care of machine-dependent optimizations

```c
#include <stdio.h>

int main()
{
    int i;
    int q, r, t, x[100000], y[100010], z[100011];

    for (i=0; i<100000; i=i+1)
    {
        x[i]= q + y[i] *(t*z[i+10] + t *z[i+11]);
        printf("%d\n", x[i]);
    }

    return 0;
}
```
ISA Independent Synthetic Benchmarks

<table>
<thead>
<tr>
<th>ISA</th>
<th>Static Code Size</th>
<th>Inst. Count</th>
<th>Cycle Count</th>
<th>IPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>x86</td>
<td>45 (18)</td>
<td>80.7M</td>
<td>68.2M</td>
<td>1.18</td>
</tr>
<tr>
<td>Sparc</td>
<td>93 (55)</td>
<td>50.8M</td>
<td>47.2M</td>
<td>1.08</td>
</tr>
<tr>
<td>Alpha</td>
<td>100(44)</td>
<td>107.4M</td>
<td>72.4M</td>
<td>1.48</td>
</tr>
</tbody>
</table>

**LLVM ISA**

```
@tmp1 = load i32* %v, align 4
@tmp2 = load i32* %v, align 4
@tmp3 = getelementptr [100000 x i32]* %v, i32 0, i32 @tmp2
@tmp4 = load i32* %v, align 4
@tmp5 = load i32* %v, align 4
@tmp6 = add 132 %tmp6, 1
@tmp7 = getelementptr [100001 x i32]* %v, i32 1, i32 0, i32 @tmp6
@tmp8 = load i32* %v, align 4
@tmp9 = load 132 %tmp9, align 4
@tmp10 = mul 132 %tmp10, %tmp9
@tmp11 = load 132 %v, align 4
@tmp12 = add 132 %tmp12, 1
@tmp13 = getelementptr [100002 x i32]* %v, i32 2, i32 0, i32 @tmp12
@tmp14 = load 132 %tmp14, align 4
@tmp15 = load 132 %v, align 4
@tmp16 = mul 132 %tmp16, %tmp15
@tmp17 = add 132 %tmp17, 1
@tmp18 = load 132 %v, align 4
@tmp19 = add 132 %tmp19, 1
```

**Alpha**

```
addq $0, $3, $3
mulq $1, $4, $1
mulq $2, $5, $2
lda $4,20($30)
ldl $3,0($3)
addq $2, $1, $1
ldl $2,0($4)
mulq $3, $1, $1
lda $3,32($30)
addq $1, $2, $1
s4addq $0, $3, $0
stl $1,0($0)
ldl $0,0($11)
s4addq $0, $3, $0
```

**Sparc**

```
sethi 4193522, %g1
add %g1, %g1
add %g1, 680, %15
smul %11, %14, %11
smul %12, %13, %12
ld [%g1+10], %13
add %12, %11, %11
sethi 4193132, %g1
add %g1, %g1
id [%g1+28], %12
smul %13, %11, %11
sethi 4193132, %g1
add %g1, %g1
add %g1, 40, %13
add %11, %12, %11
st %11, [%13+10]
sethi 4193132, %g1
add %g1, %g1
```

**x86**

```
movl 12(%esp), %eax
movl 000112(%esp,%eax,4), %ecx
imull 24(%esp), %ecx
movl 000108(%esp,%eax,4), %edx
imull 20(%esp), %edx
addl %ecx, %edx
```
Other Applications

- Generate Clones by setting knobs to appropriate values
- Adaptable
- Scalable
- Futuristic
Synthetic Benchmarks

- Performance and Power Clones for RTL
- Stress Benchmarks
- Clones for Proprietary Applications
- Benchmarks with Knobs Adjustable Benchmarks Scalable Benchmarks
- Futuristic Benchmarks
Sharing Proprietary Applications

- Military Applications cannot be shared with Vendors
- Many commercial applications cannot be shared freely between software and hardware developers

Proprietary Applications

Performance/Power Clones
Early Performance Testing

- **Usage Scenario**
  - Derive proxy applications from a set of workload characterizations
  - Proxies convey no proprietary information, but capture the execution behavior of XX’s applications
  - Proxy applications can be available very early in project
  - Proxies focus on the computationally significant portions of code, not the small parts that are hardware-dependent (e.g., DMA, etc.)

> Early testing confirms performance, or discovers shortfalls in time to address them before final integration
Proxy Applications can Transform Procurement Process

- Proxy applications can turn vendors into partners in achieving performance goals
  - Provides them with means to directly measure performance
  - Places the iterative test/analyze process in vendor’s labs
  - Reveals no proprietary information

- Turn hardware performance tuning into a supplier task
  - Periodically capture application performance in a new set of proxies
  - Task supplier to re-tune hardware for best performance as applications mature
POWER AMD THERMAL STRESSTMARKS

- Hand crafting code snippets for power viruses
  - Very tedious process, complex interactions inside the processor
  - Cannot be sure if it is the maximum case
  - Heavily architecture dependent; heavy domain knowledge

- We automatically generate power viruses

<table>
<thead>
<tr>
<th>Power Virus</th>
<th>Optimized to stress</th>
<th>Language</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPrime</td>
<td>All CPUs, all ISAs</td>
<td>C</td>
</tr>
<tr>
<td>CPUburn-in</td>
<td>X86 machines</td>
<td>x86 assembly</td>
</tr>
<tr>
<td>BurnP5</td>
<td>Intel Pentium w&amp;w/o MMX processors</td>
<td>x86 assembly</td>
</tr>
<tr>
<td>BurnP6</td>
<td>Intel PentiumPro, Pentium II, Pentium III and Celeron CPUs</td>
<td>x86 assembly</td>
</tr>
<tr>
<td>BurnK6</td>
<td>AMD K6 processors</td>
<td>x86 assembly</td>
</tr>
<tr>
<td>BurnK7</td>
<td>AMD Athlon/Duron processors</td>
<td>x86 assembly</td>
</tr>
<tr>
<td>BurnMMX</td>
<td>cache/memory interfaces on all CPUs with MMX</td>
<td>x86 assembly</td>
</tr>
</tbody>
</table>
POWER and THERMAL STRESSMARKS

- Automatically search for power viruses using an abstract workload model and machine learning

- GA: search heuristic to solve optimization problems

- Choose a random population, evaluate fitness, apply GA operators to generate next population

- Evolve until required fitness achieved
- **BurnK7** – 72.1 Watts
- **SPEC CPU2006**: 416.gamess and 453.povray consume highest power of 63.1 and 59.6 Watts
SYMPO Framework – Genetic Algorithm

- Individuals -> synthetic workloads
- Fitness function -> power on the design under study
- Mutation rate, reproduction rate, crossover rate

Single-point Crossover

Single-point Mutation
Validation on Real Hardware

- Our code generator was not equipped to generate code for x86 at that time
  - Generated power viruses on SPARC ISA and translated to x86 using LLVM infrastructure
A Solution to The Expiring Benchmark Problem

- SPEC89, SPEC92, SPEC95, SPEC CPU2000, CPU 2006
- TPC A, TPC B, TPC D
- Benchmarks become obsolete very quickly
- Benchmark makers create inflated data sets to stay alive at least 4-5 years
- Generate futuristic benchmarks using the proxy code generator
# Interactive Workloads??

High-level feature categories need to be modified for interactive properties

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Instruction-level Characteristics</td>
</tr>
<tr>
<td>2</td>
<td>Control-flow Characteristics</td>
</tr>
<tr>
<td>3</td>
<td>Memory-access Characteristics</td>
</tr>
<tr>
<td>4</td>
<td>Interactive Workload Characteristics</td>
</tr>
</tbody>
</table>
Weaknesses – The Vitamin Tablet Problem

Vitamin A, B, C, D, E, K

What about undiscovered vitamins? Vitamin P, Q, R?
Summary

• We have developed a proxy generation methodology to generate miniature proxy benchmarks.

• PerfProx proxies can enable fast and efficient performance evaluation of emerging workloads without needing back-end database or complex software stack support.

• We would like the community to use these proxies for architecture research to improve the reproducibility of the work with minimal effort.

• Automating the process will be helpful for deployment of our proxy generation tools (Intel project objective).
References

References


References


References – Past Dissertations

- Rob Bell, Ph. D Dissertation, UT Austin 2005, **Automatic Workload Synthesis for Early Design Studies and Performance**
- Ajay Joshi, Ph. D Dissertation, UT Austin 2008, **Constructing Adaptable and Scalable Synthetic Benchmarks for Microprocessor Performance Evaluation**
- Karthik Ganesan, Ph. D dissertation, UT Austin 2012, **Automatic Generation of Synthetic Workloads for Multicore Systems**
- Reena Panda, Ph. Dissertation, UT Austin 2017, **Accurate Modeling of Core and Memory Locality for Proxy Generation Targeting Emerging Applications and Architectures**
The University of Texas at Austin
lca.ece.utexas.edu
BACK UP
Branch bit vectors

- Need a lightweight way to specify taken/transition rates of a branch
  - Minimize computational overhead to avoid skewing results
- Solution: Compare a 1-hot shift register against a static 32 bit vector
  - High transition rate branches use a register that shifts every iteration
  - Low transition rate branches use a register that shifts every 32 iterations
  - Branch if zero flag not set (both vectors had a 1 in the same position)
- Examples (using short vectors):
  - 11001100: 50% taken rate, 50% transition rate (1.6% with slow shift register)
  - 11101110: 75% taken rate, 50% transition rate
  - 10101010: 50% taken rate, 100% transition rate
  - 10000000: 12.5% taken rate, 25% transition rate
Generation Process

- Generate vector with target number of transitions
  - Roughly equal-sized groups of 0s and 1s, roughly 50% taken rate

- Flip bits to match target taken rate, without impacting transition rate
  - V[n] can be flipped if V[n-1] != V[n+1]
  - Example: 11110000 and 11100000 have the same transition rate

- Randomize the vector
  - Perform a random rotation
  - Shuffle groups of bits without impacting transition rate
    - Example: 11011010 and 11010110 have the same transition rate
COMPARISON WITH STANDARD BENCHMARKS

- Cassandra-ORIG
- Cassandra-Proxy
- MongoDB-ORIG
- MongoDB-Proxy
- MySQL-ORIG
- MySQL-Proxy
- SPEC-CPU2006
- SPECJBB2013
- Linpack