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Laboratory for Computer Architecture

The Laboratory for Computer Architecture (LCA) is a research group within the Department of Electrical and Computer Engineering at The University of Texas at Austin. The lab is directed by Dr. Lizy Kurian John and is part of the Computer Engineering Research Center (CERC).

The members of the Laboratory for Computer Architecture are investigating several topics in computer architecture. Some of our current research interests include:

- Performance Impact of Contemporary Programming Paradigms
- Emerging Workloads
- Architectures for Emerging Workloads
- Workload Characterization
- Performance Modeling
- Low Power Architectures
- Architectural and Compiler Optimizations for Improving Performance and Reducing Energy

UT ECE

Fall 2005

Current Research

Performance Impact of Emerging Workloads

The growth of information technology has resulted in the proliferation of computers to every aspect of human life. In addition to scientific/technical workloads, general purpose workloads, Java, object-oriented, network processor, file-system, multi-media, database, electronic commerce, web-servers, mail-servers, graphics, speech recognition, image recognition, life sciences, pharmaceuticals, and several other categories of workloads have made into the main-stream. Research at the Laboratory for Computer Architecture (LCA) is directed at understanding the performance of these emerging applications on current architectures and developing architectural enhancements to improve their performance.

Performance and Power Modeling

Computer systems are becoming increasingly complex, both from hardware and software perspectives. Simulation, which is a very popular tool among designers takes very long due to complex hardware and long running benchmarks. This problem becomes worse during performance evaluation where a lot of data needs to analyzed. The project focuses on investigating mathematical and statistical techniques to optimize the process of simulation and reduce the effort for performance evaluation. Some of the approaches investigated include using sampling to reduce simulation time, developing synthetic benchmarks that are representative of the real world benchmarks, finding representative benchmarks in the suite to reduce simulation effort. These approaches include a very detailed characterization of workloads, development of metrics for similarity, clustering techniques and workload analysis. The techniques are useful for modeling not only performance but also of power and energy. Some of the developed clustering techniques are being used in the selection of SPEC's next suite of CPU benchmarks.

Embedded Java Acceleration

With the increasing demands placed on mobile systems for long battery life, high performance combined with the ever present need for low cost, embedded mobile systems present an fertile ground for both hardware and software enhancements.

Our work focuses on enhancing the performance of Java for mobile platforms. Architectural enhancements relating to code cache management, dynamic bytecode stream optimization, and runtime profile guided optimization are investigated. The project is funded by Samsung, Korea.

Low Power and Adaptive Architectures

Minimizing power and energy has become a necessity during design of microprocessors and computer systems. We are involved in developing hardware and software techniques to reduce and manage power consumption. One approach is to adapt the hardware to selectively use power-hungry hardware only when needed. The success of this technique depends on the ability to detect regions where hardware should be scaled up or down. We employ workload characterization and phase detection to correctly identify effective regions for power management

Faculty

Dr. Lizy Kurian John directs the Laboratory for Computer Architecture (LCA). She is an Associate professor and Engineering Foundation Centennial Teaching Fellow in the Electrical and Computer Engineering department at UT Austin. She received her Ph. D in Computer Engineering from Penn State in 1993. She has received several awards including the 2003 Texas Exes teaching award, the UT Austin Engineering Foundation Faculty award (2001), the Halliburton Young Faculty award (1999), and the NSF CAREER award. She is a member of IEEE, IEEE Computer Society, ACM, and ACM SIGARCH. She is also a member of Eta Kappa Nu, Tau Beta Pi and Phi Kappa Phi Honor Societies.

Runtime Identification of Microprocessor Energy Saving Opportunities
W. Lloyd Bircher, Madhavi Valluri, Lizy John, and Jason Law,
International Symposium on Low Power Electronics and Design. pp 275-280. August 2005

Reducing Server Data Traffic using a Hierarchical Computation Model
Juan Rubio and Lizy K. John,
IEEE Transactions on Parallel and Distributed Systems. Vol. 16. No. 10. pp 933-943. October 2005

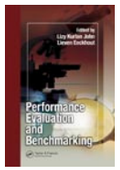
Implications of Executing Compression and Encryption Applications on General Purpose Processors
Byeong Kil Lee and Lizy K. John,
IEEE Transactions on Computers. Vol. 54. No. 7. pp 917-922. July 2005.

Locality Based On-Line Trace Compression
Yue Luo and Lizy K. John,
IEEE Transactions on Computers. Vol. 53. No. 6. pp 723-731. June 2004

Benchmarking Internet Servers on Superscalar Machines
Yue Luo, Juan Rubio, Lizy John, Pattabi Seshadri, and Alex Mericas,
IEEE Computer pp 34-40, February 2003

Simulating Commercial Java Throughput Workloads: A Case Study
Yue Luo and Lizy John,
International Conference on Computer Design (ICCD). October 2005

Evaluating MMX Technology Using DSP and Multimedia Applications
Ravi Bhargava, Lizy John, Brian L. Evans, and Ramesh Radhakrishnan,
IEEE Symposium on Microarchitecture. pp 37-46. December 1998



Performance Evaluation and Benchmarking
Lizy Kurian John ,
Lieven Eeckhout,
Taylor and Francis, CRC press

Sponsors

LCA expresses its deep gratitude to the following organizations for supporting its research.

IISWC (IEEE Intl. Symposium on Workload Characterization)

WWC (Workshop on Workload Characterization) which Dr. Lizy John organized during 1998-2004 has evolved into an IEEE International Symposium (http://www.iiswc.org)

LCA M.S Students

Hari Angepat is a Masters student who jointed the LCA group in 2004. He has a degree from Mcgill University, Canada. He is working on embedded java performance characterization and related architectural enhancements.

Jason Matalka is a Masters student in LCA. He joined LCA in 2003 and has a BS in EE from UT Austin. He is currently researching different approaches for increasing Java performance via hardware acceleration.

Sean Leather Sean Leather is pursuing a M.S. in Computer Engineering. He joined UT in 2003 after graduating from Washington University in St. Louis with a double major in Computer Engineering and Computer Science. His research involves simulation reduction and phase behavior of transaction processing workloads.

Tyler Olsen is a M.S. student who joined in August 2004. He has a B.S. in computer engineering from Purdue University. He is working on representative trace generation using phase profiling of performance monitor data.

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LCA Ph.D Graduates

Dr. Ramesh Radhakrishnan graduated from UT Austin in August 2000. He joined the Server and Storage Performance Team at Dell where his duties included performance evaluation and analysis of server and storage systems, performance projections for enterprise servers, competitive analysis, architectural tradeoff analysis and design support. Since June 2004, he has been working as a senior design engineer in Dell's High Performance Computing Team, where he is responsible for designing HPC products that achieve the raw-computing power of classic "big-iron" supercomputers using cutting-edge standardized technologies.

Dr. Deepu Talla graduated from The University of Texas with a Ph.D. in Computer Engineering in 2001. Currently, he is a System Architect in the Imaging and Audio group at Texas Instruments. He is responsible for the product and architecture definition of portable multimedia SOC He was one of the core architects of the recently announced "DaVinci (TM)" platform.

Dr. Ravi Bhargava received his Ph.D. from UT Austin in 2003. Ravi is currently a member of the server microprocessor design team at Advanced Micro Devices in Austin, Texas. His responsibilities at AMD include microarchitecture design, performance modeling, and virtualization support.

Dr. Tao Li received the Ph.D. degree in computer engineering from the University of Texas at Austin in 2004. He has been an assistant professor in the Department of Electrical and Computer Engineering at University of Florida since August 2004. He is founder and principle investigator of the Intelligent Design of Efficient Architectures Laboratory at University of Florida. His research interests include computer architecture, low power, secure and dependable computing, application-specific systems, performance evaluation, the impacts of eme-rging techniques and applications on computer designs, operating systems and compilers.

Dr. Juan Rubio received his Ph.D. from UT, Austin in August 2004. He currently works at IBM Austin Research Lab.

Dr. Madhavi Valluri obtained her PhD degree from the University of Texas at Austin in May 2005. She also holds masters degrees from the University of Texas at Austin and the Indian Institute of Science, Bangalore. Madhavi works in the Systems and Technology Group at IBM (Austin) on improving performance of general-purpose programs via code analysis. Specifically, her project focus is on exploring optimization opportunities in the POWER6 compiler and micro-architecture. Her research interests include compiler and micro-architectural techniques for high performance and low power.

Dr. Byeong Kil Lee is a microprocessor design engineer in WTBU (Wireless Terminal Business Unit) at Texas Instruments Inc. He is working on designing a high perfor-mance processor for next generation handheld devices. His research interests include performance modeling, workload, characterization, formal verification, network processor, multimedia processor and performance analysis. He received a Ph.D in computer engineering from The University of Texas at Austin in 2005.

Dr. Yue Luo is from China. He received his Master's Degree in electronics from Peking University. He joined LCA in 2000. Under Professor John's supervision, Yue Luo did research in workload characterization and microprocessor simulation methodology. He graduated with a Ph.D. degree in 2005. Yue is now working at Microsoft as a Software Development Engineer in Test. He is a member of the Reliability Team in the Windows Fundamentals group. His current project involves the safe mode and restart manager in Windows Vista.

LCA M.S Graduates

Class of 2004

Saket Kumar	AMD

Class of 2003

Michael Arukumar	Intel
Lance Karm	IBM(Austin)
Mike Clark	AMD
Patrick Peters	Intrinsity

Class of 2002

Anand Sunder Rajan	ARM Corporation
James Yang	Motorola (Austin)

Class of 2000

Vikram Godbole	Intel Corp. (Austin)
Sanjeev Ghai	IBM Corp.
Srikanth Kannan	Analog Devices Inc

Class of 1999

Jyotsna S. Kartha	Freescale (Austin)
Jody Joyner	IBM Corp.
Juan Rubio	Ph.D. at UT-Austin
Poorva Gupta	Sony
Purnima Vasudevan	PMC-Sierra

Class of 1998

Roy Shalem	Intel Corp.
Da-Chih Tang	Sun Microsystems (Sunnyvale)

Class of 1997

Yin Teh	CMU

LCA B.S Graduates

Syed M. Alam was an undergraduate research assistant in LCA during his Bachelor's studies at UT Austin. He got his B.S. in electrical engineering from the University of Texas at Austin in May 1999, S. M. and Ph.D. in electrical engineering and computer science from Massachusetts Institute of Technology in June 2001 and September 2004, respectively. He is currently working with Freescale Semiconductor. His research interests include 3D Integrated Circuits, reliability CAD, thermal modeling/analysis in ICs, and interconnect analysis.

Pattabi Seshadri got BS in electrical engineering from University of Texas at Austin and he is currently working for IBM.

Nate Little got BS in electrical engineering from University of Texas at Austin and he is currently working for Trilogy.

Selected Publications

Improved Automatic Testcase Synthesis for Performance Model Validation
Robert H. Bell, Jr. and Lizy K. John,
19th ACM International Conference on Supercomputing (ICS). June 2005.

Low Power, Low Complexity Instruction Issue Using Compiler Assistance
Madhavi Valluri, Lizy K. John, and Kathryn McKinley, 19th ACM International Conference on Supercomputing (ICS). June 2005.

Control Flow Modeling in Statistical Simulation for Accurate and Efficient Processor Design Studies
Lieven Eeckhout, Robert H. Bell, Jr., Bastiaan Stougie, Koen De Bosschere,and Lizy K. John,
International Symposium on Computer Architecture (ISCA). pp 350-361. June 2004.

Improving Dynamic Cluster Assignment for Clustered Trace Cache Processors
Ravi Bhargava and Lizy K. John,
30th International Symposium on Computer Architecture (ISCA). pp264-274. June 2003.

Run-time Modeling and Estimation of Operating System Power Consumption
Tao Li and Lizy John,
International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS). pp 160-171. June 2003.

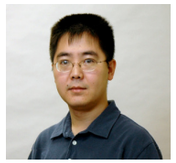
Understanding and Improving Operating System Effects in Control Flow Prediction-
Tao Li, Lizy John, Anand Sivasubramaniam, Narayanan Vijaykrishnan, and Juan Rubio,
10th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS). pp 68-80. Oct' 02.

Allowing for ILP in an Embedded Java Processor
Ramesh Radhakrishnan, Deepu Talla, and Lizy John, International Symposium on Computer Architecture (ISCA). pp 294-305. June 2000.

Architectural Issues in Java Runtime Systems
Ramesh Radhakrishnan, N. Vijaykrishnan, Lizy John, and Anand Sivasubramaniam,
International Symposium on High Performance Computer Architecture (HPCA), January 2000

LCA Ph.D. Students

Rob Bell is a Ph.D. candidate in Electrical and Computer Engineering at the University of Texas at Austin. He holds undergraduate and M.S.E.E. degrees from the University of Virginia, and is employed full-time at IBM, Austin, as a computer designer. His research interests include computer architecture, performance modeling and simulation, and representative workload synthesis.



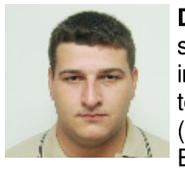
Shiwen Hu is a Ph.D. candidate at LCA. He joined LCA in 2000. Shiwen has a M.S. degree from Tsinghua University of China. Shiwen is working on efficient adaptation of multiple configurable units using dynamic optimization systems for microprocessor energy reduction.

Aashish Phansalkar is a Ph.D. candidate at Laboratory of Computer Architecture. He joined LCA in Spring 2003. He received his Bachelor's Degree in Electrical Engineering from University of Pune, India in 2000 and a Masters degree from the Department of Electrical and Computer Engineering at the University of Texas at Austin in 2002. His research interests are performance evaluation and benchmarking of microprocessors, workload characterization and computer architecture. He is currently working on techniques to measure similarity based on microarchitecture independent workload characterization of programs.

Ajay Joshi is a PhD student at LCA. He joined LCA in Fall 2003. He holds a MS degree in Electrical and Computer Engineering from Ohio State University. He is currently working on evaluating and developing techniques for generating representative synthetic workloads.

Lloyd Bircher is a Ph.D. student at LCA. He joined LCA in 2002 and has a Bachelor of Science degree in Electrical Engineering from the University of Texas at Arlington. He is currently working in the area of Software Directed Power Management for Microprocessors.

Ciji Isen is a Ph.D. student at LCA. He joined LCA in Fall of 2005 and has a Masters degree from Texas A&M University. He is currently working on characterization of embedded java benchmarks and microarchitectural techniques to enhance performance of java in embedded systems.



Dimitris Kaseridis is a Ph.D. student at UT and joined LCA in Fall 2005. He has a Masters (2005) and Diploma (2004) degree in Computer Engineering and Informatics from the University of Patras, Greece. Dimitris is working on Performance Evaluation & Analysis of Multithreaded Multiprocessor Systems. His other research interests are high performance microprocessor design and low power microarchitectures.