KARTHIK GANESAN, PhD., MS., B.E.

Senior Member, Oracle
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Education

2009 – 2011

Doctor of Philosophy at the University of Texas at Austin, USA
Thesis title: Automatic Generation of Synthetic Workloads for Multicore Systems
Department: Electrical and Computer Engineering, GPA: 3.95/4.0
Lab: Laboratory for Computer Architecture (http://lca.ece.utexas.edu)
Advisor: Dr. Lizy K John

2006 – 2008

Master of Science at the University of Texas at Austin, USA
Track: Computer Engineering, ECE department, GPA: 3.87/4.0
Relevant courses: Computer Architecture, Computer Performance Evaluation and Benchmarking, Superscalar Microprocessors, Principles of Computer Architecture, Computer Architecture – User System Interplay, Distributed Systems, Advance Compiler Techniques, Statistics for Engineers, Data mining and Collaborative Software Design

2002 – 2006

Bachelor of Engineering, Anna University, India
Department: Computer Science and Engineering, GPA – 84/100
Honors: First class with Distinction
Relevant Courses: Computer architecture I & II, Computer Graphics, Parallel computer architecture, Operating Systems, Programming and Data Structures, Compilers, DBMS & System software, Object Oriented Programming & Software Engineering

Professional Experience

Jan '12 – present

Senior Member at Oracle America. – Research involves working on performance characterization and optimization of advanced processor architectures in the Performance and Applications Engineering (PAE) department. Also, **principal investigator** on research project with the University of Texas at Austin with a **half yearly grant of 70,000 dollars from Oracle Labs**.

May '11 – August '11

Performance Architect Intern at ARM Inc. - Worked with both system level simulators and RTL level ARM processor models to research the performance of parallel workloads PARSEC and SPLASH-2 on multicore ARM processors to aid in identifying performance bottlenecks of future ARM designs.

May '08 – August '08

Research Intern at IBM Austin – Research involved work with the open source tool called Performance Inspector and was involved in implementing a patented solution by patching the kernel for solving the buffer overflow problem by dynamically slowing down the application based on buffer occupancy.

May '07 – August '07

Research Intern at IBM T. J. Watson Labs, BlueGene Design Team - Was involved in the design and validation of the novel Performance Monitoring Unit of the then world's fastest super computer, BlueGene/P and published the work in ICPP 2008, ISPASS 2008.

Academic Research

Fall '06 – Present

Research Assistant in the Laboratory for Computer Architecture, UT Austin- Worked with Prof. Lizy K John and published in peer reviewed conferences about designing a framework to distill the characteristics that are significant in terms of performance and power consumption of modern parallel and sequential workloads into synthetic benchmarks to help in the pre-silicon design stage of computer systems. The framework was also leveraged to generate power viruses for a given processor design using machine learning.

May '04 – July '06

Undergraduate Part-time Research Trainee, Waran Research Foundation, India - Was working in the High Performance Architecture Group "Viswakarma" in designing a novel Memory In Processor (MIP) architecture, which culminated into the thesis, titled "Hierarchical Multihost based Operating System for Simultaneous Multiple Application Execution on Memory In Processor Super Computer On Chip Cluster" focusing on a novel silicon operating system design for clusters.

Refereed Publications

- Karthik Ganesan and Lizy K John, "Automatic Generation of Miniaturized Synthetic Proxies for Target Applications to Efficiently Design Multicore Processors" in IEEE Transactions on Computers, 2013.
- Karthik Ganesan, "Automatic Generation of Synthetic Workloads for Multicore Systems", Department of Electrical and Computer Engineering, The University of Texas at Austin, Dec 2011.
- Karthik Ganesan and Lizy K John, "MAximum Multicore POwer (MAMPO) - An Automatic Multithreaded Synthetic Power Virus Generation Framework for Multicore Systems" as **best paper finalist** in the SuperComputing Conference (SC 2011), Seattle, WA, Nov 2011.
- Karthik Ganesan, J. Jo, W. L. Bircher, D. Kaseridis, Z. Yu and Lizy K John, "System-level Max Power (SYMPO) – A systematic approach for escalating system-level power consumption using synthetic benchmarks" at the 19th Intl. conf. on Parallel Architectures and Compilation Techniques (PACT), Vienna, Austria, Sep 2010.
- Karthik Ganesan, Jungho Jo, Lizy K John, "Synthesizing Memory-Level Parallelism Aware Miniature Clones for SPEC CPU2006 and ImplantBench Workloads" at 2010 IEEE International Symposium on Performance Analysis of Systems and Software, New York, March 2010.
- Karthik Ganesan. Lizy K. John, James Sexton, and Valentina Salapura. "A Performance Counter Based Workload Characterization on Blue Gene/P " at the 37th International conference on parallel processing, ICPP 2008 at Portland, Oregon, Sep 2008. (In collaboration with IBM T J Watson Labs)
- Valentina Salapura, Karthik Ganesan, Alan Gara, Michael Gschwind, James C. Sexton, and Robert E. Walkup. "Next-Generation Performance Counters: Towards Monitoring Over Thousand Concurrent Events", presented at the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2008), April 2008. (In collaboration with IBM T J Watson Labs)
- Karthik Ganesan, Deepak Panwar, and Lizy John. "Generation, Validation and Analysis of SPEC CPU2006 Simulation Points Based on Branch, Memory, and TLB Characteristics" In 2009 SPEC Benchmark Workshop. Austin, Texas, January 2009 and also submitted as Master's report to the University of Texas at Austin in 2008.
- Lizy John, Jungho Jo and Karthik Ganesan, "Workload Synthesis for a Communications SoC", In Workshop on SoC Architecture, Accelerators and Workloads, held in conjunction with HPCA-17, San Antonio, Texas, Feb 2011
- Venkateswaran Nagarajan, Karthik Ganesan et al "Future Generation Supercomputers II: A Paradigm for Cluster Architecture" in ACM SIGARCH Computer Architecture News, Vol. 35, No. 5, December 2007.

- Venkateswaran Nagarajan, Karthik Ganesan et al "On the Concepts of Simultaneous Execution of Multiple Applications on the Hierarchically based Cluster and the Silicon Operating System" selected for presentation at the 22nd IEEE International Parallel and Distributed Processing Symposium, IPDPS 2008, Miami, in Apr '08.

- Karthik Ganesan, "Hierarchical Multihost Based Operating System For Simultaneous Multiple Application Execution on MIP SCOC Cluster", undergraduate thesis submitted to Waran Research Foundation (WARFT), 2006.

- N.Venkateswaran, Karthik Ganesan et al "High Performance Low Power Single Chip Reconfigurable Supercomputer for High-end Aerospace Applications" Selected for presentation at the 8th International MAPLD 05 Conference conducted by NASA on Sep 7, 2005. The above given paper was also presented in the Birds Of Feather Workshop on Sep 8, 2005 in MAPLD 2005.

- N.Venkateswaran, Karthik Ganesan et al "Simulation Model for predicting The Multi-Million Neuron Interconnectivity and Evolution of a Neurophysiologically Inspired Supercomputing Architecture for Modeling the Respective Brain Regions" Presented at Max Planck Institute of Medical Research Workshop, "Data driven Modeling and Computational Neuroscience" DMCN 2005, Heidelberg, Germany, conducted by Prof Bert Sakmann, Nobel Laureate 1991, Springer Verlag.

- Karthik Ganesan and Vishwanath Venkatesan, "Emulating IBM BlueGene on a Linux MPI Cluster", undergraduate final year project submitted to Anna University, 2006.

Teaching & Mentoring

Fall '06, Sp & Fall '07	**Teaching Assistant** for the course "Digital design using VHDL" involving programming using VHDL and FPGA Implementation using Modelsim and Xilinx.
Fall '07	**Teaching Assistant** for the course "Superscalar Microprocessor Architectures" involving various simulations for different superscalar processor microarchitectures.
Fall '10	**Mentored full time undergraduate student**, Mr. Vincent Davis through UT's Summer Research Academy 2010 program organized by Texas Research Experience (TREX) for the project titled "Synthesizing Clones for the Most Optimal SPEC CPU2006 Simulation Point"

Technical Skills

Programming Languages/Knowledge	JAVA • C • C++ • PHP • Shell Programming • Matlab • Perl • Oracle/SQL • VB 6.0/VB Script • Cell Processor programming • Alpha/SPARC/PowerPC/ARM assembly • CUDA GPU programming • Sequoia parallel programming language
Operating Systems	Basic to advance user skills in Linux • Basic user skills in Solaris, Windows, Mac OS X and Android
Hardware Description Languages	VHDL • Verilog
Performance Evaluation Tools	PIN • SimpleScalar • Wattch • HLS • Simics • Multifacet GEMS • Orion • SPEC CPU suites • Mibench • ImplantBench • PARSEC suite • Splash-2 suite • DRAMsim • Cacti
Software Tools Developed/Worked on	Multithreaded Synthetic Benchmark Generator – Multithreaded synthetic benchmark generation framework for performance, power analysis of Multicore systems • Simpoints for SPEC CPU2006 Alpha Binaries • IBM Performance Inspector – http://perfinsp.sourceforge.net/
Other skills	Good team player, excellent problem solving and communication skills

System Administration	System administrator for the Laboratory for Computer Architecture and the Archer grid infrastructure for computer architecture research and education at the University of Texas at Austin.

Awards and Honors

- Was awarded the honorable mention to the **SPEC distinguished dissertation award** at the ACM/SPEC International Conference on Performance Engineering (ICPE 2013) at Prague, Czech Republic.
- **Oracle Atta Award** for JVM performance on SPARC within one year after joining Oracle from the director of Performance and Application Engineering.
- **Best Project Award** for the final year undergraduate project titled "Emulating IBM BlueGene On Linux MPI Cluster" among all of 2006 graduates.
- One of the two **Best paper finalists** out of 352 high quality papers received at the Supercomputing conference (SC 2011).
- **Invited paper** to the Journal of Scientific Programming, by the chief editor from Oxford, UK and also to the journal Advances in Software Engineering.
- **NSF PACT Travel grant** to present at PACT 2010
- **ISPASS Travel grant** to present a paper at the ISPASS 2010
- Won the **University of Texas at Austin Professional Development Awards** thrice for paper presenation and technical excellence in Sep 2010, Nov 2011 and Apr 2008
- **Graduate Engineering Council Travel Grant** to present paper at IEEE PACT 2010
- Graduated with **First Class & Distinction** from the department of Computer Science and Engineering, Anna University in 2006.
- **Best paper presentation award** at the IBM sponsored inter-collegiate event Prajna '05, Chennai, India.

Professional Service

- **Technical Advisory Committee member** of the International Conference on Pattern Recognition Applications and Techniques (ICPRAT 2013)
- **Technical reviewer** for Transactions on Computers, Supercomputing Conference (SC 2011), TACO 2011, PACT 2010, IEEE MICRO 2011, ISCA 2012
- **Developer of the open sourced** Simpoint Proxies for SPEC CPU2006 Alpha binaries
- Member of the Standard Performance Evaluation Corporation (SPEC) Research group
- Member of IEEE, ACM, SIGPLAN, USENIX
- A representative for Oracle America Inc at the Standard Performance Evaluation Corporation (SPEC)
- Volunteer at the Supercomputing Conference (SC 2009)