# Estimation of Intrinsic Small Signal Parameters of a GaAs MESFET from DC Measurements

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**ABSTRACT**

This investigation offers a technique to predict the AC behavior of mm wavelength GaAs metal semiconductor field effect transistors (MESFETs) by using DC characteristics. To predict the intrinsic equivalent circuit parameters of the device from DC data, the measured DC characteristics are first simulated by employing a non-linear DC model. The effects of biasing on the device AC parameters are evaluated for its low-noise applications. An improvement greater than 10% in predicting the AC response of the device is observed. The concept of depletion layer modification caused by the transverse electric field inside the channel is introduced for accurate Miller's capacitor modeling. It is assumed that with increased device biasing there are more unbalanced positive ionic charges in the gate depletion towards the drain-side of the Schottky barrier. The electric field lines originated by these uncompensated charges induce an opposite charge density in the gate electrode. This modifies the gate biasing and hence the Schottky barrier depletion. As a result, the values of intrinsic AC device parameters change. It is observed that an accurate DC modeling is a key to predict an accurate AC small signal equivalent circuit of a device.

**1- INTRODUCTION**

Unipolar devices are inherently faster compared to bipolar devices. This primarily is attributed to the high mobility of carriers in the materials that are employed for the fabrication of unipolar devices [1,2]. GaAs metal semiconductor field effect transistors (MESFETs) with submicron channel length can operate comfortably at a frequency greater than 100 GHz. Whereas modulation doped field effect transistors (MODFETs) can give the frequency range much greater than what is observed in MESFETs, i.e., > 500 GHz [3,4]. The designing of an AC prober at such a high frequency is exceptionally a difficult task. Usually, the range of a prober is much lower than the expected device maximum frequency of oscillation. And the device full AC capabilities are predicted by experimental extrapolation technique [5,6].

Furthermore, with the available on wafer AC probing, the accurate measurements are linked with a high degree of calibration and the evaluation is not a straightforward process as that of DC measurements. From industrial point of view such complications may affect the throughput and thus a technique that can predict the AC behavior of the device from DC characteristics would be a beneficial one. Utilization of DC data for device parameter extraction process give quick realization of its AC capabilities. But with conventional analysis, in which ideal device characteristics are assumed, DC data does not describe the microwave characteristics of a device to an acceptable accuracy. This discrepancy further enhances when the device size reduces to submicron regimes. In such cases, the observed mismatch between the predicted and measured AC response is primarily attributed to the short channel effects observed in submicron devices [7,8].

In this article a technique has been developed which can predict the AC response of short channel devices to an acceptable accuracy by using DC characteristics. The output and the transfer characteristics of the device are first evaluated. By employing a non-linear DC model, the observed characteristics are then simulated with an optimization algorithm. Once a good fit is attained the model is then extended to predict the AC response of the device. The developed technique thus covers the discrepancy which arises due to short

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channel effects namely: a) significant output conductance in the saturation region of operation; b) shift in threshold voltage; c) its dependency on drain-to-source biasing and d) compression in transconductance. The variations in Miller's capacitor values, which define the upper limit of the bandwidth of a device, have been evaluated as a function of applied biasing. And the same has been explained by assuming a depletion modification caused by perpendicular electric field underneath the Schottky barrier gate. The developed technique takes into account the 2nd order effects [9,10] which are usually there in submicron devices and thus gives an accurate prediction of AC intrinsic small signal parameters. The technique on one hand gives a good accuracy in the predicted parameters it, on the other hand, is a simple one which provides an efficient handling for circuit designing that involves short channel MESFETs.

**Nomenclature**

| | |
|---|---|
| $\alpha, \lambda, \gamma$ | empirical constants |
| $N$ | channel doping density |
| $q$ | electronic charge |
| $\varepsilon_s$ | permittivity of GaAs |
| $\Phi_b$ | Schottky barrier potential |
| $h$ | depletion height |
| $L_g$ | gate length |
| $\upsilon_s$ | saturation velocity |
| $W$ | gate width |
| $a$ | channel height |
| $V_T$ | threshold voltage |
| $\Delta V_T$ | shift in threshold voltage |
| $L_{sg}$ | source-to-gate spacing |
| $L_{gd}$ | gate-to-drain spacing |
| $X$ | extension of gate depletion |
| $E_{pi}$ | epitexial layer thickness |
| $\mu_n$ | mobility of electron |
| $V_{gs}$ | gate-to-source voltage |
| $V_{ds}$ | drain-to-source voltage |
| $I_{ds}$ | drain-to-source current |
| $C_{gs}$ | gate-to-source capacitance |
| $C_{gd}$ | gate-to-drain capacitance |
| $C_{ds}$ | drain-to-source capacitance |
| $C_p$ | pad capacitance |
| $R_s$ | source resistance |
| $R_d$ | drain resistance |
| $R_c$ | ohmic contact resistance |
| $R_i$ | channel resistance |
| $g_d$ | output conductance |
| $g_m$ | transconductance |
| $f_T$ | transition frequency |
| $\tau$ | charging delay |

## 2- MESFET's MODEL

For submicron GaAs MESFETs, $I_{ds}(V_{gs}, V_{ds})$ characteristics may be simulated by employing the following relationship [11,12]

$$I_{ds} = qNaWv_s\left[1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right]^2 \times \tanh(\alpha V_{ds})(1 + \lambda V_{ds}) \quad (1)$$

where $$V_T = \frac{qNa^2}{2\varepsilon_s}, \quad (2)$$

and $$\Delta V_T = \frac{4a}{3L_g} V_T \quad (3)$$

In Fig. (1), the simulated and the observed characteristics of a 200 nm long and 4 x 25 $\mu$m wide device are shown. A reasonably good fit shows that the Eqn. (1) could be used with its optimized empirical constants to predict the changed Schottky barrier response with changing values of gate biasing. The device under investigation was chosen such that it shows a deviation from its ideal response. That is, shift in $V_T$ from its theoretical value, compression in $g_m$ and a high value of $g_d$. These 2nd order effects may be attributed to the finite surface state density at Schottky barrier [13-15] which generates a discrepancy between the observed and expected AC response of the device. Such effects are not easy to predict because they are associated with unpredictable surface states at the Schottky barrier interface. Practically, these 2nd order effects may be incorporated in the subsequent modeling once a good match has been attained in the observed and simulated data. So instead of predicting the device response from its theoretical assumed values the simulated $I_{ds}(V_{gs}, V_{ds})$ characteristics can be employed to asses its AC behaviour.

By involving the simulated $I_{ds}(V_{gs}, V_{ds})$ characteristics, the magnitude of $C_{gs}$ and $C_{gd}$ may be estimated by using the following

expressions [1,16,17]

$$C_{gs} = \varepsilon_s L_g W\left[a - \frac{I_{ds}(V_{gs}, V_{ds})}{qNv_s W}\right]^{-1} \quad (4)$$

$$C_{gd} = \frac{\varepsilon_s L_g W}{h(V_{gs}, V_{ds})} \quad (5)$$

where

$$h = \left[\frac{2\varepsilon_s\left(V_{ds1} - V_{gs} + \Phi_b\right)}{qN}\right]^{1/2} \quad (6)$$

and

$$V_{ds1} = V_{ds} - I_{ds} \times (R_d + R_s) \quad (7)$$

Knowing the device geometry and $R_c$ the values of $R_s$ and $R_d$ can be determined

$$R_s = \frac{L_{sg}}{qN\mu_n WE_{pi}} + R_c \quad (8)$$

$$R_d = \frac{(L_{gd} - X)}{qN\mu_n WE_{pi}} + R_c \quad (9)$$

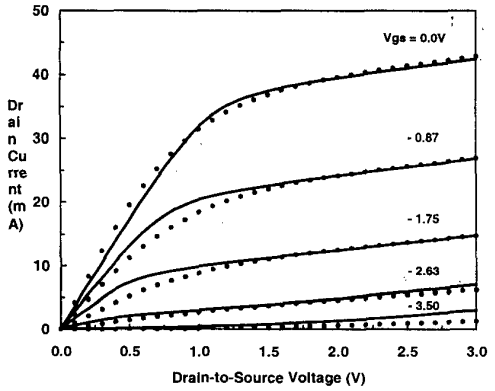



FIG. (1) Shows the simulated and observed output characteristics of 200 nm long and 100 $\mu$m wide interdigitated GaAs MESFET.

In Eqn. (4) and (5) had $C_{gs}$ and $C_{gd}$ been evaluated by using the ideal values of $I_{ds}$ and $h$ the predicted response would always be different from the observed one. Examining Eqn. (4) and (7) it is evident that for the evaluation of $C_{gs}$ and $C_{gd}$ the simulated value $I_{ds}(V_{gs},V_{ds})$ is used instead of its ideal value. This compensates the observed 2nd order effects in all subsequent evaluation in which $I_{ds}$ is a variable. Thus the predicted AC response of the device will be closer to the experimental observations.

Fig. (2) shows the variation in $C_{gs}$ as a function of $V_{gs}$ for a fixed value of $V_{ds}$. It is obvious from the plot that the modified method for the evaluation of $C_{gs}$ differs significantly from first order approximate approach where $I_{ds}$ is assumed as a constant parameter after the onset of current saturation.

The simulated values of $C_{gs}$ and $C_{gd}$ as a function of device biasing are shown in Fig. (3). Examination of the figure reveals that $C_{gs}$ shows an increase whilst $C_{gd}$ exhibits a decrease with increasing values of $V_{ds}$. By increasing $V_{ds}$ there is an extension in the Schottky barrier depletion towards the drain side of the device. As a result the capacitance value of $C_{gd}$ decreases as seen in Fig. (3-b). The electric field lines originated by the positive ionic charges of the extended depletion will have their maximum strength near the drain side of the gate electrode. It is assumed that negative charges are induced in the gate metal, because of these field lines, resulting in a reduction in the gate biasing [18]. This decreases the gate depletion and hence increases $C_{gs}$ as illustrated in Fig. (4). Increased value of $C_{gs}$ reduces the high frequency capability of a transistor and this effect is, usually, not incorporated in first order AC performance prediction models. Moreover, the plot shows that at usual low-noise amplifier biasing the value of $C_{gs}$ = 20 fF whereas $C_{gd}$ = 35 fF. This indicates that $C_{gd}$ has significant contribution in the Miller's capacitors evaluation and thus cannot be ignored for short channel devices [2].

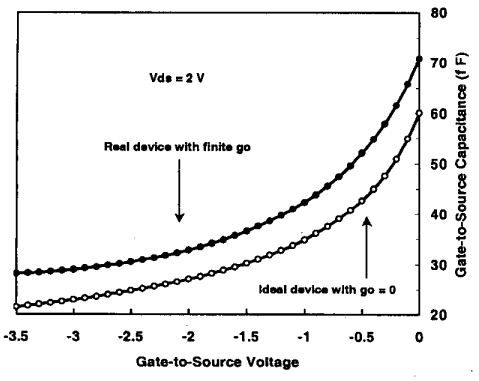



FIG. (2) Shows the difference between the values of gate-to-source capacitance of a GaAs MESFET calculated by new technique (solid circle) in comparison with the conventional technique (open circle).

The value of $C_{ds}$ that depends on the depletion height and the device geometry may be estimated by using the following expression.

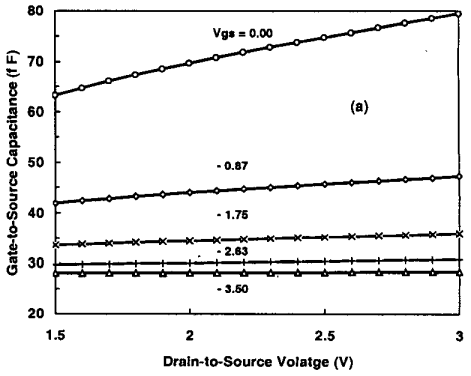
$$C_{ds} = \frac{\varepsilon_s h(V_{gs}, V_{ds})W}{L_g} \qquad (10)$$

The estimated values of $C_{ds}$ as a function of $V_{gs}$ are shown in Fig. (5). As expected the $C_{ds}$ capacitor is at least on tenth of $C_{gs}$. An increase in the capacitance value by increasing the gate potential could be explained on the basis of increased depletion height which eventually defines the physical size of $C_{ds}$.

In short channel device the most unpredictable parameter is $g_d$ [10]. It could be simulated at various biasing to a reasonable accuracy by differentiating Eqn. (1)

$$g_d = \left(1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)\left(\frac{\gamma V_{gs}}{(V_T + \Delta V_T + \gamma V_{ds})^2}\right)$$

$$\times \tanh(\alpha V_{ds})(1 + \lambda V_{ds})(2qnav_s W)$$



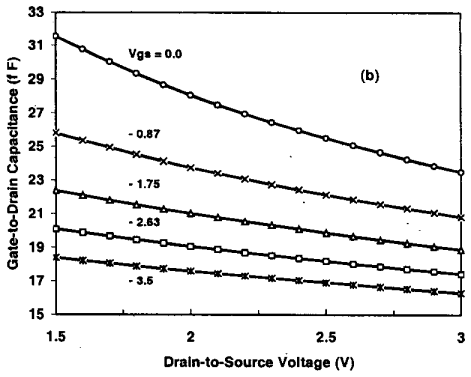




FIG. (3) Represents (a) gate-to-source capacitance (b) gate-to-drain capacitance as a function of applied bias of a submicron GaAs MESFET

$$+\left(1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)^2 \left[1 - \tanh^2(\alpha V_{ds})\right]$$

$$\times(1 + \lambda V_{ds})(2qnav_s W)\,\alpha$$

$$+\left(1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)^2 \tanh(\alpha V_{ds})$$

$$\times(2qnav_s W)\lambda \qquad (11)$$

Fig. (6) shows the simulated values of $g_d$ of a submicron MESFET. The variation in $g_d$ as a function of $V_{gs}$ and $V_{ds}$ is attributed to the change in $\alpha$-$h$ value. An increase in $y$-directed

field lines reduces the gate depletion which controls the effective

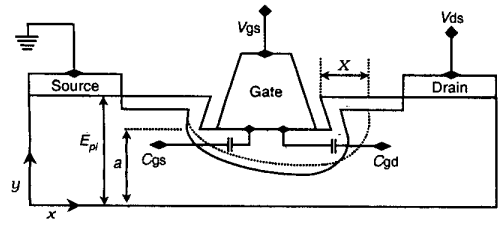



FIG. (4) A crossectional view of a GaAs MESFET illustrating the modification of its depletion with changing values of $V_{ds}$.

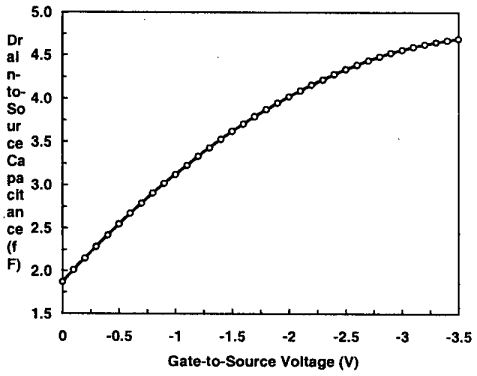



FIG. (5) Variation of drain-to-source capacitance of a 200 nm long GaAs MESFET at $V_{ds}$ = 2V.

channel height for the flow of current. An increase in effective channel height in the saturation region of operation increases the $I_{ds}$ and hence the output characteristics show a positive slope in that region.

The value of $g_m$ by using Eqn. (1) is represented by

$$g_m = \left[1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right] 2qNa v_s W$$

$$\times \left[\frac{\tanh(\alpha V_{ds})(1 + \lambda V_{ds})}{V_T + \Delta V_T + \gamma V_{ds}}\right] \qquad (12)$$

Combining Eqn. (2), (3) and (6) yields

$$f_T = \frac{g_m}{(C_{gs} + C_{gd} + Cp)2\pi} \qquad (13)$$

And the magnitude of $\tau$ is calculated by

$$\tau = \frac{C_{gs} + C_{gd}}{g_m} \qquad (14)$$

The variation in Eqn. (12), (13) and (14) as a function of applied bias is shown in Fig. (7). The maximum value of $f_T$ observed from the plot is about 37 GHz, where $\tau \sim 4.3$ psec and $g_m \sim$ 16.0 mS.

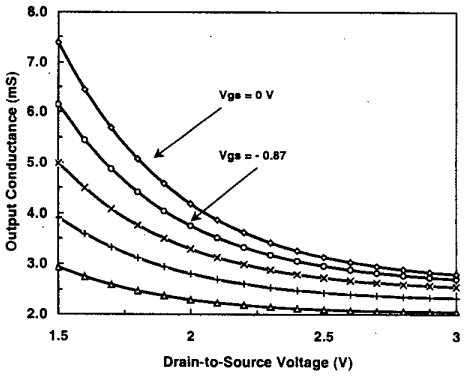



FIG. (6) Output conductance vs applied biasing for 200 nm long and 100 $\mu$m wide interdigitated MESFET.

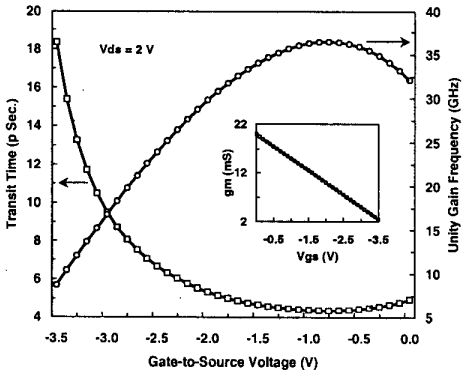



FIG. (7) Illustrates change in transit frequency along with the transit time. Inset shows the device transconductance as a function of gate potential.

Ignoring the observed 2nd order effects the value of $f_T$ is in the range of 50 GHz. This clearly shows that there will be a significant mismatch in the observed and predicted AC response of the device.

Another AC parameter that could be affected by the presence of 2nd order effects is the value of

$R_i$ which can be evaluated by using the following expression

$$R_i = \frac{v_s L_g}{I_{ds}(V_{gs}, V_{ds})} \qquad (15)$$

Variation in $R_i$ as function of $V_{gs}$ with a fixed value of $V_{ds}$ is shown in Fig. (8). The plot shows an exponential increase in $R_i$ because the channel crossection is decreasing by increasing $V_{gs}$ and hence $R_i$ is increasing. Since the change in $h$ ($V_{gs}$) is not a linear function so does $R_i$. Keeping $N$ and $a$ constant, a high value of $R_i$ means that

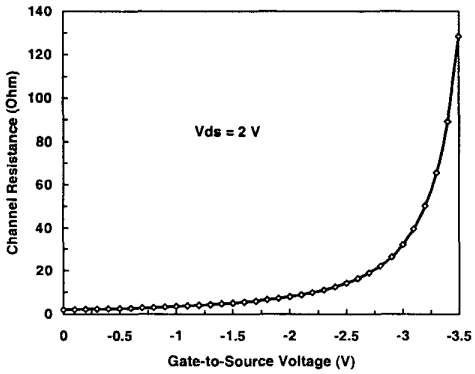



FIG. (8) Channel resistance vs gate biasing for a fixed value of drain potential of a submicron GaAs MESFET.

the device is operated near threshold region. But maintaining all these parameters constant, a discrepancy in $R_i$ value may be attributed to the 2nd order effects in the device which are of significant nature and cannot be overlooked.

### 3- ESTIMATED AC BEHAVIOR

Selecting the $Q$ point approximately at $I_{dss}/5$, the biasing voltage would be $V_{ds}$ = 2 V and $V_{gs}$ = -1.7 V. The intrinsic small signal equivalent circuit parameters with the developed technique are then evaluated and presented in Table 1. The estimated value of $f_T$ for the device under consideration is about 33 GHz, whereas the conventional approach predicts the estimated value of $f_T$ = 49 GHz.

The calculated error shown in Table-1 is consistent and could be explained on the basis of depletion movement as a function of applied potential. The highest discrepancy is observed in the value of $R_i$. This is so because in modeling usually interfacial properties of the Schottky barrier are overlooked [19,20]. The device under investigation is operated at $V_{gs}$ = -1.7 V. The gate potential, excluding the gate source drop, is consumed in moving the depletion toward the substrate hence it reduces the available channel height for the flow of current. As a result, the channel resistance increases. Whenever the device exhibits the non ideal characteristics, which is usually there, part of the applied potential is consumed by the interfacial oxide layer and hence the depletion movement is relatively slow. Consequently, the available channel for the flow of carriers is large and the channel resistance is small. Due to the slow nature of interface states such devices will have negative impact on AC signals, hence the high frequency capabilities of the device is deteriorated to a considerable extent.

To predict the AC response of a device, it is important to know the exact nature of its Schottky barrier quality. It is not possible to evaluate the surface state density and thus there may be ambiguity in the predicted values of intrinsic equivalent circuit parameters. This uncertainty could be removed if the device DC output characteristics are first simulated to a reasonable accuracy with experimental data and then all subsequent AC evaluation should be made on the basis of simulated DC characteristics. It is observed that key to a successful prediction from DC data is an accurate DC simulation of output characteristics, especially in the saturation region of operation.

| Elements | New Technique | Conventional Technique | % Error |
|---|---|---|---|
| $R_i$ | 6.0 Ω | 37.1 Ω | 83.8 |
| $g_d$ | 3.29 mS | 2.8 mS | 14.8 |
| $g_m$ | 11.5 mS | 14.4 mS | 20.0 |
| $\tau$ | 4.9 pSec | 3.2 pSec | 34.7 |
| $C_{gs}$ | 34.5 fF | 28.8 fF | 16.5 |
| $C_{gd}$ | 21.0 fF | 18.0 fF | 14.28 |
| $C_{ds}$ | 3.80 fF | 4.5 fF | 15.5 |

Table-1 Intrinsic equivalent circuit parameters of a 200 nm long and 100 $\mu$m wide GaAs MESFET at biasing voltage $V_{ds}$ = 2V and $V_{gs}$ = -1.7V.

## 4- CONCLUSION

A technique has been developed to predict accurately AC intrinsic small signal parameters of a submicron GaAs MESFET by using its DC characteristics. The device DC behavior is first observed and then by using a non-linear DC model the experimental data is simulated by an optimization algorithm. All subsequent AC evaluations are based on the simulated data which take into account the 2nd order effects which are usually present in submicron devices. It is shown that if these effects are not considered then there could be a significant discrepancy in the predicted AC behavior. Furthermore, Variation in device intrinsic capacitors values as a function of $V_{ds}$ in saturation region of operation has been explained on the basis of depletion modification caused by transverse electric field lines. This reduces the applied gate biasing and as result gate depletion shrinks to a new value. It is also observed that in submicron devices $C_{gd}$ has comparable value with $C_{gs}$ at optimum bias point for small signal applications and therefore cannot be ignored. The developed technique provides an efficient way to predict the AC response of the device and could be a useful tool for circuit simulation software that involves submicron GaAs MESFETs.

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