



Laboratory for Computer Architecture



The Laboratory for Computer Architecture (LCA) is a research group within the Department of Electrical and Computer Engineering at The University of Texas at Austin. The lab is directed by Dr. Lizy Kurian John and is part of the Computer Engineering Research Center (CERC).

The members of the Laboratory for Computer Architecture are investigating several avenues in computer architecture. Some of our current research interests include:

- Cloud and Big Data Architecture
- Memory Systems for Multicore and Many-core Architectures
- Workload Characterization
- Proxies for Computer Performance/Power Evaluation
- Low Power Architectures
- Development of Energy-efficient, High-Performance Codes
- Compiler Support for Innovative Micro-architectures



Cloud and Big Data Architecture

Analyzing massive amounts of data, deriving insight and seeing things one could not see before has become important for businesses, medicine, world economy and human life in general. It is important that next generation computer systems handle these analytics workloads efficiently. Our studies will attempt to understand emerging big data computing workloads to drive hardware and software development.



Memory Systems for Multicore Architectures

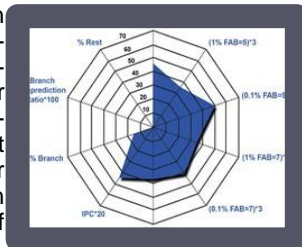


As microprocessors move from the multi-core to the many-core era, the Von Neumann memory bottleneck is becoming more critical. For instance, the SPARC server platform roadmap (2010 to

2015) projects a 32X increase in the number of threads in 5 years. To be able to leverage such abundant computing power, it is important to design efficient memory subsystems. We are currently looking at different memory configurations, hierarchies and data partitioning algorithms that can minimize the number of off-chip (or off-node) memory accesses and/or minimize the latencies observed by the processing unit.

Workload Characterization

Workload characterization and identification of bottlenecks allows computer architects to design computer systems that yield high performance, energy-efficient operation and reliability. Our research group focuses on workload characterization of emerging application domains and emerging processor architectures. Understanding the nature of programs and the workload behavior leads to the design of improved computer architectures.



Proxies for Performance/Power Evaluation

We are working on creating proxy workloads for big data and cloud workloads. Our research also includes creation of power, reliability and thermal stressmarks that help to identify guard-bands in design. We develop automated procedures to develop benchmarks and stressmarks that test and validate modern computer systems from performance, power, energy, thermal and reliability perspectives.



Development of Energy-efficient, High-Performance Codes

Among the many hurdles faced in research and development of compute-intensive codes is achieving high performance and energy efficiency. We work with computational scientists to identify bottlenecks in their codes as they execute on modern computer systems. Algorithms created by computational scientists will be analyzed and optimizations to improve performance and energy-efficiency incorporated. We perform thorough evaluations of high performance codes and co-design the codes to explore alternative algorithm/hardware scenarios.



Compiler Support for Microarchitectures

Our research in this area focuses primarily on identifying mechanisms that will allow compilers to provide hints to the microarchitecture in order to increase its efficiency and maximize the performance. We are currently looking at the tradeoffs of data prefetching and bus utilization, as well as compiler support for innovative mechanisms such as the VBBI Indirect Branch Predictor and SLB Branch Predictor.



Faculty



Dr. Lizy Kurian John directs the Laboratory for Computer Architecture (LCA). She holds the B. N. Gafford Professorship and is an Engineering Foundation Centennial Teaching Fellow in the Electrical and Computer Engineering department at UT Austin. She has received several awards including the Texas Exes teaching award, the UT Austin Engineering Foundation Faculty award, the Halliburton Young Faculty award, the NSF CAREER award, UT Alumni Association Teaching award, and the Penn State University Outstanding Engineering Alumnus award. She is an IEEE fellow, a senior member of IEEE Computer Society, and a member of ACM, ACM SIGARCH, Eta Kappa Nu, Tau Beta Pi and Phi Kappa Phi Honor Societies.

LCA Ph.D. Students



Maithili Gandhe is a Ph.D. student in LCA. Her research interests are dynamic power management, ubiquitous computing, user-based power/performance optimization, etc.

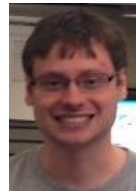


Jungho Jo is a Ph.D. student and joined the LCA in Spring 2008. He also received his MS degree at UT. He is currently working on ISA independent synthetic benchmarks for early design stage analysis.



Jee Ho Ryoo is a Ph.D. student at UT and joined LCA in Fall 2011. He received his M.S degree from University of Texas at Austin. He is

currently working on analysis and design of memory scheduling policies.



workloads.

Michael LeBeane is a Ph.D. student who joined LCA in Fall 2013. He received his undergraduate degrees from Washington University in St. Louis and is currently working on characterizing big data and cloud



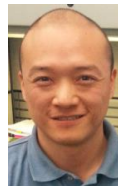
Reena Panda joined UT Austin Fall 2013. Before joining UT, she received my Masters in Computer Engineering from Texas A&M University in Fall 2011. Her research interests lie in big-data workload characterization/ modeling and core micro-architecture.



Jiajun Wang is a Ph.D. student who joined LCA Spring 2014. She is currently working on HPC workloads analysis and optimization.



Ahmed Khawaja is a Ph.D student and joined LCA Spring 2014. His research interests are architecture bottleneck identification.



Wooseok Lee is a Ph.D. student. He received his M.S. degree from INHA University, Korea. His research interests are improving energy efficiency of heterogeneous system and power modeling of processor.



Shuang Song is a Ph.D student. He joined LCA in Fall 2014. He is now working on performance and power characterization of TPCx-HS.

LCA Ph.D Graduates



Dr. Youngtaek Kim received his Ph.D. from UT in Spring 2013. His research included automatic test and management of voltage noise in microprocessor power distribution networks. He currently works at AMD.



Dr. Arun Nair graduated with his Ph.D. in May 2012. His research was in the areas of architectural vulnerability and reliability. He is currently employed as a performance architect at AMD.



Dr. Umar Farooq graduated with his Ph.D. in spring 2013. His research interests include compiler and micro-architecture interaction. His thesis work was on guided power aware ILP extraction and branch prediction.



Dr. Faisal Iqbal received his Ph.D from UT in August 2013. His research interests included multi-core power/performance optimization, network processing and hard-ware accelerators.



Dr. Dimitris Kaseridis received his Ph.D. from UT in May 2011. He joined LCA in Fall 2005. He has a Masters (2005) and Diplo-ma (2004) degree in Computer Engineering and Informatics from the University of Patras, Greece.

Dimitris worked on design, performance evaluation & analysis of multithreaded multicore systems along with high performance microprocessor design. He is currently working at ARM.



Dr. Jian Chen received his Ph.D. in May 2011. He joined LCA in Summer 2006. He received his MS degree in electrical engineering from Shanghai Jiao Tong University, China. He worked on power aware microarchitectures for

multi-cores and models for such systems. He is currently working at Intel.



Dr. Jeff Stuecheli received his Ph.D. in May 2011. He joined LCA in 2000. He has worked full time at IBM Austin in microprocessor development since 1997. His research interests include cache hierarchy, CMP, coherence, performance/power analysis/optimization, and benchmarking.



Dr. Ciji Isen received the Ph.D. in May 2011. He joined LCA in Fall of 2005 and has a Masters degree from Texas A&M University. He worked on improving memory systems using memory state knowledge. He joined AMD in 2011.



Dr. Karthik Ganesan received his Ph.D. from UT Austin in December 2011. He joined LCA in Fall 2006. He holds a BE in Computer Science and Engineering (2006) from Anna University during which he was a Part time research trainee at Waran Research Foundation, India. He worked on Performance Evaluation of High performance Multiprocessor Systems. He is currently working at Oracle.



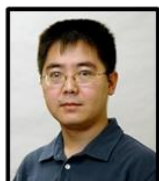
Dr. Lloyd Bircher received his Ph.D. in December 2010. He joined LCA in 2002 and has a Bachelor of Science in Electrical Engineering from the University of Texas at Arlington and a Master of Science in Computer Engineering from the University of Texas at Austin. He worked in the area of software directed power management of microprocessor systems. He is currently at AMD.



Dr. Ajay Joshi graduated with a Ph. D in December 2007. His research was on synthetic bench-marks, especially stress bench-marks for power and thermal evaluation. He currently works for ARM.



Dr. Aashish Phansalkar graduated with a Ph. D in 2007 May. His research centered on similarity analysis of workloads. He currently works for Intel. Before that he worked for Marvel Technologies.



Dr. Shiwen Hu received his Ph.D. in 2005. He joined LCA in 2000. Shiwen has a M.S. degree from Tsinghua University of China. Shiwen's dissertation was on efficient adaptation of multiple configurable units using dynamic optimization systems for microprocessor energy reduction. He is currently employed at Freescale.



Dr. Rob Bell received his Ph.D from the University of Texas at Austin in 2005. He holds under-graduate and M.S.E.E. degrees from the University of Virginia, and is employed full-time at IBM, Austin, as a computer designer. His research interests include computer architecture, performance modeling and simulation, and representative workload synthesis.



Dr. Yue Luo received his Master's Degree in electronics from Peking University. Under Professor John's supervision, Yue Luo did research in workload characterization and microprocessor simulation methodology. He graduated with a Ph.D. degree in 2005. Yue is now working at Microsoft as a Software Development Engineer in Test.



Dr. Byeong Kil Lee is currently Vice President at Samsung. He is working on designing a high performance processor for next generation handheld devices. His research interests include performance modeling, workload, characterization, formal verification, network -processor, multimedia processor and performance analysis. He received a Ph.D in computer engineering from UT Austin in 2005.



Dr Madhavi Valluri obtained her Ph.D. degree from the University of Texas at Austin in May 2005. Madhavi works in the Systems and Technology Group at IBM (Austin) on improving performance of general-purpose programs via code analysis. Her research interests include compiler and micro-architectural techniques for high performance and low power.



Dr. Juan Rubio received his Ph.D. from UT, Austin in August 2004. He currently works at IBM Austin Research Lab.



Dr. Tao Li received the Ph.D. degree in computer engineering from the University of Texas at Austin in 2004. He is now an associative professor in the Department of Electrical and Computer Engineering at University of Florida. His research interests include computer architecture, low power, secure and dependable computing, application-specific systems, performance evaluation, the impacts of emerging techniques and applications on computer designs, operating systems and compilers.



Dr. Ravi Bhargava received his Ph.D. from UT Austin in 2003. Ravi is currently a member of the server microprocessor design team at Advanced Micro Devices in Austin, Texas. His responsibilities at AMD include microarchitecture design, performance modeling, and virtualization support.



Dr. Deepu Talla graduated from The University of Texas with a Ph.D. in Computer Engineering in 2001. Currently he is Vice President and General Manager of the Mobile Business Unit at NVIDIA. He was at Texas Instruments for 10 years before joining NVIDIA. He is responsible for the product and architecture definition of portable multimedia SOC. He was one of the core architects of the recently announced "DaVinci (TM)" platform.



Dr. Ramesh Radhakrishnan graduated from UT Austin in August 2000. Since June 2004, he has been working as a senior design engineer in Dell's High Performance Computing Team, where he is responsible for designing HPC products that achieve the raw-computing power of classic "big iron" super-computers using cutting-edge standardized technologies. Currently he serves as Technologist at the Office of the CTO, Dell.

LCA M.S Graduates

Class of 2013

Donald Owen	Sandia National Labs
Ankita Garg	Nvidia

Class of 2011

Bhargavi Narayanasetty	Intel
Chaitanya Nayak	

Class of 2008

Rajiv Bhatia	IBM
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Class of 2007

Justin Friesenhahn	IBM
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Class of 2006

Jason Matalka	Centaur
Lloyd Bircher	Ph.D at UT-Austin

Class of 2005

Brian Gaide	Xilinx
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Class of 2004

Saket Kumar	AMD
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Class of 2003

Michael Arukumar	Intel
Lance Karn	IBM(Austin)
Mike Clark	AMD
Patrick Peters	Intrinsity

Class of 2002

Anand Sunder Rajan	ARM Corporation
James Yang	Motorola (Austin)

Class of 2000

Vikram Godbole	Intel Corp. (Austin)
Sanjeev Ghai	IBM Corp.
Srikanth Kannan	Analog Devices Inc

Class of 1999

Jyotsna S. Kartha	Freescale (Austin)
Jody Joyner	IBM Corp.
Juan Rubio	Ph.D. at UT-Austin
Poorva Gupta	Sony
Purnima Vasudevan	PMC-Sierra

Class of 1998

Roy Shalem	Intel Corp.
Da-Chih Tang	Sun Microsystems (Sunnyvale)

Class of 1997

Yin Teh	CMU
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LCA B.S Graduates

Sara Bird	UC Berkeley
Syed M. Alam	Freescale
Pattabi Seshadri	IBM Corp.
Nate Little	Trilogy
Santos Gomez	Amazon

Selected Publications

Performance Analysis of HPC Applications with Irregular Tree Data Structures

Ahmed Khawaja, Jiajun Wang, Dhairya Malhotra, Andreas Gerstlauer, George Biros and Lizy John. The 20th IEEE International Conference on Parallel and Distributed Systems. December 2014

Control Flow Behavior of Cloud Workloads

Jee Ho Ryoo, Michael LeBeane, Muhammad Faisal Iqbal, and Lizy K. John. The IEEE International Symposium on Workload Characterization (IISWC) (Poster). October 2014.

FastSpot: Host-Compiled Thermal Estimation for Early Design Space Exploration

Darshan Gandhi, Andreas Gerstlauer, and Lizy K. John. The 15th IEEE International Symposium on Quality Electronic Design (ISQED). March 2014.

Performance Boosting under Reliability and Power Constraints

Youngtaek Kim, Lizy K. John, Indrani Paul, Srilatha Manne, and Michael Schulte. The 34th IEEE/ACM International Conference on Computer-Aided Design (ICCAD). November 2013.

Flow Migration on Multicore Network Processors: Load Balancing While Minimizing Packet Reordering

Muhammad Faisal Iqbal, Jim Holt, Jee Ho Ryoo, Gustavo de Veciana, and Lizy K. John. The 42th IEEE International Conference on Parallel Processing (ICPP). October 2013.

Store-Load Branch (SLB) Predictor: A Compiler Assisted Branch Prediction for Data Dependent Branches

Muhammad Umar Farooq, Khubaib, and Lizy K. John. The 19th IEEE International Symposium on High Performance Computer Architecture. March 2013.

AUDIT: Stress Testing the Automatic Way

Youngtaek Kim, Sanjay Pant, Srilatha Manne, Michael Schulte, Lloyd Bircher, Madhu Saravana Sibi Govindan, and Lizy K. John. The 45th International Symposium on Microarchitecture (MICRO'45). December 2012.

A First-Order Mechanistic Model for Architectural Vulnerability Factor

Arun A. Nair, Stijn Eyerma, Lieven Eeckhout, and Lizy K. John. The 39th International Symposium on Computer Architecture (ISCA-39). June 2012.

Power and Performance Analysis of Network Traffic Prediction Techniques

Muhammad Faisal Iqbal and Lizy K. John. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS). April 2012.

Minimalist Open-page: A DRAM Page-mode Scheduling Policy for the Many-core Era (Best Paper Nominee)

Dimitris Kaseridis, Jeffrey Stuecheli, and Lizy K. John. 44th International Symposium on Microarchitecture (MICRO'44). December 2011.

MAXimum Multicore Power (MAMPO) - An Automatic Multithreaded Synthetic Power Virus Generation Framework for Multicore Systems (Best Paper Nominee)

Karthik Ganesan and Lizy K. John, Super Computing Conference (SC 2011). November 2011.

Coordinating DRAM and Last-Level-Cache Policies with the Virtual Write Queue

Jeff Stuecheli, Dimitris Kaseridis, David Daly, Hillery Hunter, Lizy K. John, IEEE Micro, Special Issue on the Top Picks from the Computer Architecture Conferences, January/February 2011.

AVF Stressmark: Towards an Automated Methodology for Bounding the Worst-case Vulnerability to Soft Errors

Arun A. Nair, Lizy K. John, and Lieven Eeckhout, 43rd International Symposium on Microarchitecture (MICRO'43). December 2010.

Elastic Refresh: Techniques to Mitigate Refresh

Penalties in High Density Memory

Jeff Stuecheli, Dimitris Kaseridis, David Daly, Hillery Hunter, and Lizy K. John, 43rd International Symposium on Microarchitecture (MICRO'43). December 2010.

System-level Max Power (SYMPO) - A Systematic Approach for Escalating System Level Power Consumption Using Synthetic Benchmarks

Karthik Ganesan, Jungho Jo, W. Lloyd Bircher, Dimitris Kaseridis, Zhibin Yu, and Lizy K. John, 19th International Conference on Parallel Architecture and Compilation Techniques (PACT). September 2010.

The Virtual Write Queue: Coordinating DRAM and Last-Level Cache Policies

Jeff Stuecheli, Dimitris Kaseridis, David Daly, Hillery Hunter, and Lizy K. John, 37th International Symposium on Computer Architecture (ISCA). June 2010.

Bandwidth-aware Memory-subsystem Resource Management using Non-invasive Resource Profilers for Large CMP Systems

Dimitris Kaseridis, Jeffrey Stuecheli, Jian Chen, and Lizy K. John, 16th International Symposium on High-performance Computer Architecture (HPCA). January 2010.

Value Based BTB Indexing (VBBI) for Indirect Jump Prediction (Best Paper Nominee)

Muhammad Umar Farooq, Lei Chen, and Lizy K. John, 16th International Symposium on High-Performance Computer Architecture (HPCA). January 2010.

Knowledge of Inconsequential Memory Occupancy for DRAM subsystem

Ciji Isen and Lizy K. John, 42nd International Symposium on Microarchitecture (MICRO). December 2009.

Automated Microprocessor Stressmark Generation

Ajay Joshi, Lieven Eeckhout, Lizy K. John, and Ciji Isen, 14th International Symposium on High Performance Computer Architecture (HPCA). February 2008.

Analysis of Redundancy and Application Balance in the SPEC CPU2006 Benchmark Suite

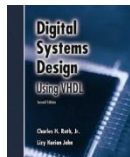
Aashish Phansalkar, Ajay Joshi, and Lizy K. John, 34th International Symposium on Computer Architecture (ISCA). June 2007.

Books



Performance Evaluation and Benchmarking

Lizy Kurian John, Lieven Eeckhout
Taylor and Francis, CRC press, 2005



Digital Systems Design using VHDL

Charles H. Roth and Lizy Kurian John,
Thomson, 2007

Sponsors

LCA expresses its deep gratitude to the following organizations for supporting its research.



IISWC (IEEE Intl. Symposium on Workload Characterization)



Dr. Lizy John founded WWC (Workshop on Workload Characterization) which has evolved into IISWC now. For more information, see the IISWC website (www.iiswc.org)



