Laboratory for Computer Architecture

The Laboratory for Computer Architecture (LCA) is a research group within the Department of Electrical and Computer Engineering at The University of Texas at Austin. The lab is directed by Dr. Lizy Kurian John and is part of the Computer Engineering Research Center (CERC).

The members of the Laboratory for Computer Architecture are investigating several avenues in computer architecture. Some of our current research interests include:

- Performance Impact of Contemporary Programming Paradigms
- Emerging Workloads
- Architectures for Emerging Workloads
- Workload Characterization
- Performance Modeling
- Low Power Architectures
- Architectural and Compiler Optimizations for Improving Performance and Reducing Energy

UT ECE

Spring 2012

Current Research

Multicore System Design and Optimization

Multicore computer systems are commonplace in embedded systems to servers. Our research focuses on designing multicore systems and optimizing them for performance, power, energy and reliability. The last level caches in these multicores are typically shared between the different cores. In our past research, we worked on cache partitioning mechanisms based on application behavior, appropriately allocating cache capacity to different applications. Another topic of interest is application scheduling based on workload characterization in heterogeneous multicores. Models for estimating performance and energy consumption of applications were developed to guide the application scheduling, in a dynamic fashion. Another area of interest is multicore power management. Power management heuristics based on application phases are developed and used to guide operating systems in performing power-aware optimizations.

Performance Modeling and Workload Synthesis

Computer systems are becoming increasingly complex, both from hardware and software perspectives. Cycle accurate simulation models are prohibitively time-consuming, limiting the amount of design tradeoff analysis that can be performed in early design stages. In LCA, we have been working on low cost models that can be used in early design analysis. Recent research focused on generating performance and power proxies for long workloads/benchmarks. Our methodology is to perform workload characterization, capture essential features, and then create a miniaturized proxy (clone) which has the same performance and power characteristics as the original workload. Our clones can be simulated with detailed cycle accurate simulators in a quick fashion, consuming 3 or 4 orders less time than the original workload. This methodology can also be used to create proxies for proprietary applications. For instance, if a military or proprietary commercial application cannot be shared with a hardware developer, our cloning methodology can be used to create a proxy without divulging the original code or functionality. The workload synthesis methodology can further be extended to create power stress marks, thermal stressmarks, reliability stressmarks, etc.

Performance Impact of Emerging Workloads

The growth of information technology has resulted in the proliferation of computers to every aspect of human life. purpose workloads, Java, object-oriented, In addition to scientific/technical workloads, general network processor, file-system, multi-media, database, electronic commerce, web-servers, mail-servers, graphics, speech recognition, image recognition, life sciences, pharmaceuticals, and several other categories of workloads have made into the main-stream. Research at the Laboratory for Computer Architecture (LCA) is directed at understanding the performance of these emerging applications on current architectures and developing architectural enhancements to improve their performance.

Low Power and Adaptive Architectures

Minimizing power and energy has become a necessity during design of microprocessors and computer systems. We are involved in developing hardware and software techniques to reduce and manage power consumption. One approach is to adapt the hardware to selectively use power-hungry hardware only when needed. The success of this technique depends on the ability to detect regions where hardware should be scaled up or down. We employ workload characterization and phase detection to correctly

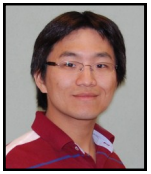
Faculty

Dr. Lizy Kurian John directs the Laboratory for Computer Architecture (LCA). She is an Associate professor and Engineering Foundation Centennial Teaching Fellow in the Electrical and Computer Engineering department at UT Austin. She received her Ph.D. in Computer Engineering from Penn State in 1993. She has received several awards including the 2003 Texas Exes teaching award, the UT Austin Engineering Foundation Faculty award (2001), the Halliburton Young Faculty award (1999), and the NSF CAREER award. She is a member of IEEE, IEEE Computer Society, ACM, and ACM SIGARCH. She is also a member of Eta Kappa Nu, Tau Beta Pi and Phi Kappa Phi Honor Societies.

LCA Ph.D. Students

Umar Farooq is a PhD student who joined LCA in Spring 2007. He received his MS(ECE) from UT-Austin in Fall 2006. His area of research is compiler and micro-architecture interaction. Currently he working on compiler guided power aware ILP extraction and branch prediction

Arun Nair joined UT Austin and LCA in Fall 2006 to pursue a Ph.D. He has received a masters degree from the University of California, Irvine and a BS from the University of Bombay, India. He is working on architectural vulnerability and reliability



Jungho Jo is a Ph.D. student and joined the LCA in Spring 2008. He also received his MS degree at UT. He is currently working on ISA independent synthetic benchmarks for early design stage analysis.

Youngtaek Kim is a PhD student and joined LCA in Spring 2009. He received his BS/MS degrees from Hanyang University, South Korea. His research interests are reliability on multi-core processors, communication architecture such as bus and NoC, and system-level design methodology for SoC design. He is currently working on automatic test and management of voltage noise in microprocessor power distribution networks.

Faisal Iqbal is a Ph.D. student in LCA. His research interests include multi-core power/performance optimization, network processing, hardware accelerators, etc.

Maithili Gandhe is a Ph.D. student in LCA. Her research interests are dynamic power management, ubiquitous computing, user-based power/performance optimization, etc.

Jee Ho Ryoo is a Ph.D. student at UT and joined LCA in Fall 2011. He received his B.S. degree from Cornell University. He is currently working on analysis and design of memory scheduling policies.

LCA Ph.D Graduates

Dr. Karthik Ganesan received his Ph.D. from UT Austin in December 2011. He joined LCA in Fall 2006. He holds a BE in Computer Science and Engineering (2006) from Anna University during which he was a Part time research trainee at Waran Research Foundation, India. He worked on Performance Evaluation of High performance Multiprocessor Systems. He is currently working at Oracle.

Dr. Ciji Isen received the Ph.D. in May 2011. He joined LCA in Fall of 2005 and has a Masters degree from Texas A&M University. He worked on improving memory systems using memory state knowledge. He joined AMD in 2011.

Dr. Dimitris Kaseridis received his Ph.D. from UT in May 2011. He joined LCA in Fall 2005. He has a Masters (2005) and Diploma (2004) degree in Computer Engineering and Informatics from the University of Patras, Greece. Dimitris worked on design, performance evaluation & analysis of multithreaded multicore systems along with high performance microprocessor design. He is currently working at ARM.

Dr. Jian Chen received his Ph.D. in May 2011. He joined LCA in Summer 2006. He received his MS degree in electrical engineering from Shanghai Jiao Tong University, China. He worked on power aware microarchitectures for multi-cores and models for such systems. He is currently working at Intel.

Dr. Jeff Stuecheli received his Ph.D. in May 2011. He was a part-time graduate student and joined LCA in 2000. He has a Bachelor of Science and Master of Science in Computer Engineering from the University of Texas at Austin. He has worked full time at IBM Austin in microprocessor development since 1997. His research interests include cache hierarchy, CMP, coherence, performance/power analysis/optimization, and benchmarking.

Dr. Lloyd Bircher received his Ph.D. in December 2010. He joined LCA in 2002 and has a Bachelor of Science in Electrical Engineering from the University of Texas at Arlington and a Master of Science in Computer Engineering from the University of Texas at Austin. He worked in the area of software directed power management of microprocessor systems. He is currently at AMD.

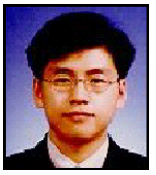
Dr. Ajay Joshi graduated with a Ph. D in December 2007. His research was on synthetic benchmarks, especially stress benchmarks for power and thermal evaluation. He currently works for Intel.

Dr. Aashish Phansalkar graduated with a Ph. D in 2007 May. His research centered on similarity analysis of workloads. He currently works for Intel. Before that he worked for Marvel Technologies.

Dr, Shiwen Hu received his Ph.D. in 2005. He joined LCA in 2000. Shiwen has a M.S. degree from Tsinghua University of China. Shiwen's dissertation was on efficient adaptation of multiple configurable units using dynamic optimization systems for microprocessor energy reduction. He is currently employed at Freescale.

Dr. Rob Bell received his Ph.D from the University of Texas at Austin in 2005. He holds undergraduate and M.S.E.E. degrees from the University of Virginia, and is employed full-time at IBM, Austin, as a computer designer. His research interests include computer architecture, performance modeling and simulation, and representative workload synthesis.

Dr. Yue Luo is from China. He received his Master's Degree in electronics from Peking University. He joined LCA in 2000. Under Professor John's supervision, Yue Luo did research in workload characterization and microprocessor simulation methodology. He graduated with a Ph.D. degree in 2005. Yue is now working at Microsoft as a Software Development Engineer in Test. He is a member of the Reliability Team in the Windows Fundamentals group. His current project involves the safe mode and restart manager in Windows Vista.



Dr. Byeong Kil Lee is an assistant professor at UT San Antonio. He is working on designing a high performance processor for next generation handheld devices. His research interests include performance modeling, workload, characterization, formal verification, network - processor, multimedia processor and performance analysis. He received a Ph.D in computer engineering from The University of Texas at Austin in 2005.

Dr. Madhavi Valluri obtained her Ph.D. degree from the University of Texas at Austin in May 2005. She also holds masters degrees from the University of Texas at Austin and the Indian Institute of Science, Bangalore. Madhavi works in the Systems and Technology Group at IBM (Austin) on improving performance of general-purpose programs via code analysis. Specifically, her project focus is on exploring optimization opportunities in the POWER6 compiler and micro-architecture. Her research interests include compiler and micro-architectural techniques for high performance and low power.

Dr. Juan Rubio received his Ph.D. from UT, Austin in August 2004. He currently works at IBM Austin Research Lab.

Dr. Tao Li received the Ph.D. degree in computer engine-ering from the University of Texas at Austin in 2004. He has been an assistant profe-ssor in the Department of Electrical and Computer Engineering at University of Florida since August 2004. He is founder and principle investigator of the Intelligent Design of Efficient Architectures Laboratory at University of Florida. His research interests include computer arch-itecture, low power, secure and dependable computing, application-specific systems, performance evaluation, the impacts of emerging techniques and applications on computer designs, operating systems and compilers.

Dr. Ravi Bhargava received his Ph.D. from UT Austin in 2003.Ravi is currently a member of the server microprocessor design team at Advanced Micro Devices in Austin, Texas. His responsibilities at AMD include microarchitecture design, performance modeling, and virtualization support.

Dr. Deepu Talla graduated from The University of Texas with a Ph.D. in Computer Engineering in 2001. Currently, he is a System Architect in the Imaging and Audio group at Texas Instruments. He is responsible for the product and architecture definition of portable multimedia SOC He was one of the core architects of the recently announced "DaVinci (TM)" platform.

Dr. Ramesh Radhakrishnan graduated from UT Austin in August 2000. He joined the Server and Storage Performance Team at Dell where his duties included performance evaluation and analysis of server and storage systems, performance projections for enterprise servers, competitive analysis, architectural tradeoff analysis and design support. Since June 2004, he has been working as a senior design engineer in Dell's High Performance Computing Team, where he is responsible for designing HPC products that achieve the raw-computing power of classic "big-iron" supercomputers using cutting-edge standardized technologies.

LCA M.S Graduates

Class of 2011

Bhargavi Narayanasetty	Intel
Chaitanya Nayak	

Class of 2008

Rajiv Bhatia	IBM

Class of 2007

Justin Friesenhahn	IBM

Class of 2006

Jason Matalka	Centaur
Lloyd Bircher	Ph.D at UT-Austin

Class of 2005

Brian Gaide	Xilinx

Class of 2004

Saket Kumar	AMD

Class of 2003

Michael Arukumar	Intel
Lance Karm	IBM(Austin)
Mike Clark	AMD
Patrick Peters	Intrinsity

Class of 2002

Anand Sunder Rajan	ARM Corporation
James Yang	Motorola (Austin)

Class of 2000

Vikram Godbole	Intel Corp. (Austin)
Sanjeev Ghai	IBM Corp.
Srikanth Kannan	Analog Devices Inc

Class of 1999

Jyotsna S. Kartha	Freescale (Austin)
Jody Joyner	IBM Corp.
Juan Rubio	Ph.D. at UT-Austin
Poorva Gupta	Sony
Purnima Vasudevan	PMC-Sierra

Class of 1998

Roy Shalem	Intel Corp.
Da-Chih Tang	Sun Microsystems (Sunnyvale)

Class of 1997

Yin Teh	CMU

LCA B.S Graduates

Sara Bird	UC Berkeley
Syed M. Alam	Freescale
Pattabi Seshadri	IBM Corp.
Nate Little	Trilogy

Selected Publications

Minimalist Open-page: A DRAM Page-mode Scheduling Policy for the Many-core Era (Best Paper Nominee)
Dimitris Kaseridis, Jeffrey Stuecheli, and Lizy K. John, 44th International Symposium on Microarchitecture (MICRO'44). December 2011.

MAximum Multicore POwer (MAMPO) - An Automatic Multithreaded Synthetic Power Virus Generation Framework for Multicore Systems (Best PapernoNonee)
Karthik Ganesan and Lizy K. John, SuperComputing Conference (SC 2011). November 2011.

Coordinating DRAM and Last-Level-Cache Policies with the Virtual Write Queue
Jeff Stuecheli, Dimitris Kaseridis, David Daly, Hillery Hunter, Lizy K. John, IEEE Micro, Special Issue on the Top Picks from the Computer Architecture Conferences, January/February 2011.

AVF Stressmark: Towards an Automated Methodology for Bounding the Worst-case Vulnerability to Soft Errors
Arun A. Nair, Lizy K. John, and Lieven Eeckhout, 43rd Interenational Symposium on Microchitecture (MICRO'43). December 2010.

Elastic Refresh: Techniques to Mitigate Refresh Penalties in High Density Memory
Jeff Stuecheli, Dimitris Kaseridis, David Daly, Hillery Hunter, and Lizy K. John, 43rd Interenational Symposium on Microchitecture (MICRO'43). December 2010.

System-level Max Power (SYMPO) - A Systematic Approach for Escalating System Level Power Consumption Using Synthetic Benchmarks
Karthik Ganesan, Jungho Jo, W. Lloyld Bircher, Dimitrics Kaseridis, Zhibin Yu, and Lizy K. John, 19th International Conference on Parallel Architecture and Compilation Techniques (PACT). September 2010.

The Virtual Write Queue: Coordinating DRAM and Last-Level Cache Policies
Jeff Stuecheli, Dimitris Kaseridis, David Daly, Hillery Hunter, and Lizy K. John, 37th Interenational Symposium on Computer Architecture (ISCA). June 2010.

Bandwidth-aware Memory-subsystem Resource Management using Non-invasive Resource Profilers for Large CMP Systems
Dimitris Kaseridis, Jeffrey Stuecheli, Jian Chen, and Lizy K. John, 16th International Symposium on High-performance Computer Architecture (HPCA). January 2010.

Value Based BTB Indexing (VBBI) for Indirect Jump Prediction (Best Paper Nominee)
Muhammad Umar Farooq, Lei Chen, and Lizy K. John, 16th Interenational Symposium on High-Performance Computer Architecture (HPCA). January 2010.

ESKIMO - Energy Savings using Semantic Knowledge of Inconsequential Memory Occupancy for DRAM subsystem
Ciji Isen and Lizy K. John, 42nd International Symposium on Microarchitecture (MICRO). December 2009.

Automated Microprocessor Stressmark Generation
Ajay Joshi, Lieven Eeckhout, Lizy K. John, and Ciji Isen, 14th International Symposium on High Performance Computer Architecture (HPCA) . February 2008.

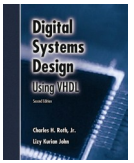
Analysis of Redundency and Application Balance in the SPEC CPU2006 Benchmark Suite
Aashish Phansalkar, Ajay Joshi, and Lizy K. John, 34th International Symposium on Computer Architecture (ISCA) . June 2007.

Experiments with the SPEC CPU 2006 Benchmark Suite: An Analysis of Redundancy and Application Balance, Aashish Phansalkar, Ajay Joshi, Lizy K. John, 34th International Symposium on Computer Architecture (ISCA), June 2007.

Improved Automatic Testcase Synthesis for Performance Model Validation
Robert H. Bell, Jr. and Lizy K. John, 19th ACM International Conference on Supercomputing (ICS). June 2005.

Books

Performance Evaluation and Benchmarking
Lizy Kurian John , Lieven Eeckhout
Taylor and Francis, CRC press, 2005



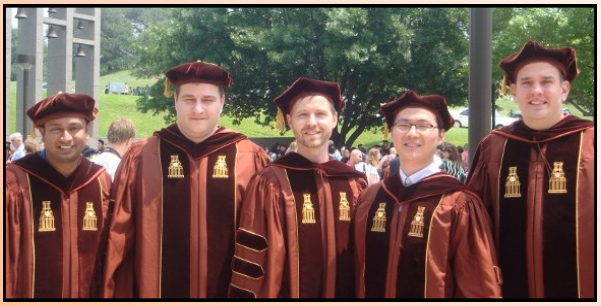
Digital Systems Design using VHDL
Charles H. Roth and Lizy Kurian John, Thomson, 2007

Sponsors

LCA expresses its deep gratitude to the following organizations for supporting its research.

IISWC (IEEE Intl. Symposium on Workload Characterization)

Dr. Lizy John founded WWC (Workshop on Workload Characterization) which has evolved into IISWC now. For more information, see the IISWC website (www.iiswc.org)



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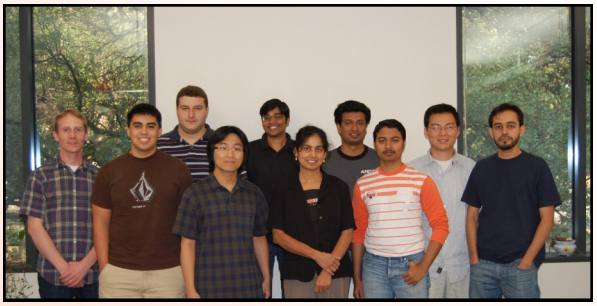

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